

# INTERNATIONAL RECTIFIER

## 2N1792, 2N1805, 2N1909, 2N2023 SERIES

### 110 Amp RMS SCRs

#### Major Ratings and Characteristics

	2N1792 thru 2N1804	2N1805 thru 2N1907	2N1909 thru 2N1916	2N2023 thru 2N2030	Units
$I_T$ (RMS)	110	110	110	110	A
$I_T$ (AV) @ $T_C$	70*	70*	70*	70*	A
$T_C$	65*	62*	85*	85*	°C
$I_{TSM}$ @ 50 Hz	955	955	955	955	A
@ 60 Hz	1,000*	1,000*	1,000*	1,000*	A
$I_{2t}$ @ 50 Hz	4,550	4,550	4,550	4,550	A <sup>2s</sup>
@ 60 Hz	4,150	4,150	4,150	4,150	A <sup>2s</sup>
$I_{GT}$	70	70	70	70	mA
$dv/dt$	200	200	50	50	V/ $\mu$ s
$di/dt$	100	100	100	100	A/ $\mu$ s
$T_J$	65* to 125*	40* to 125*	65* to 150*	65* to 150*	°C
$V_{RRM}, V_{DRM}$ range	50* to 1,200*	25* to 840*	25* to 400*	25* to 400*	V

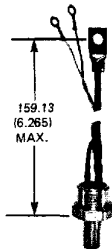
\*JEDEC registered values

#### Description/Features

- For general purpose phase control applications
- Forward and reverse voltage ratings up to 1200V
- High temperature series
- High surge rating
- Standard 1/2" ~ 20 stud
- Can be supplied as JAN and JAN-TX devices in accordance with MIL-S-19500/203 or MIL-S-19500/204.

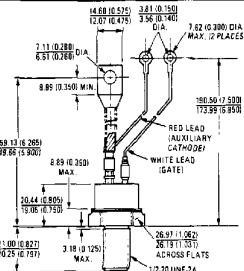
\*JEDEC registered values.

#### CASE STYLE AND DIMENSIONS

159.13  
(6.265)  
MAX.

Case style (ceramic) A-11  
furnished when part is  
rated 1000V or higher.  
A-13 (glass) for parts  
below 1000V.

JAN and/or JAN/TX  
types available.



Refer to Page A-34  
for flag terminal  
Case Style

All Dimensions in  
Millimeters and (inches)

IR Case Style A-13  
Conforms to JEDEC Outline TO-209AC (TO-94)

## VOLTAGE RATINGS (Applied gate voltage zero or negative)

Part Numbers			$V_{RRM}$ - Max. Repetitive Peak Reverse Voltage (V)	$V_{DRM}$ - Max. Repetitive Peak Off-State Voltage (V) <sup>①</sup>	$V_{RSM}$ - Max. Non-Repetitive Peak Reverse Voltage $t_p < 5$ ms (V)
TO-208AD Case	TO-209AC Case	TO-209AC Case	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$T_J = 25^\circ\text{C to } 125^\circ\text{C}$
-	2N1809	2N2023	25*	25*	35*
2N1792	2N1810	2N2024	50*	50*	70*
2N1793	2N1811	2N2025	100*	100*	150*
2N1794	2N1812	2N2026	150*	150*	225*
2N1795	2N1813	2N2027	200*	200*	300*
2N1796	2N1814	2N2028	250*	250*	350*
2N1797	2N1815	2N2029	300*	300*	400*
2N1798	2N1816	2N2030	400*	400*	500*
2N1799	2N1805	-	800*	800*	625*
2N1800	2N1806	-	720*	600*	750*
2N1801	2N1807	-	840*	700*	880*
2N1802	-	-	960*	800*	1000*
2N1803	-	-	1080*	900*	1130*
2N1804	-	-	1200*	1000*	1250*

## ELECTRICAL SPECIFICATIONS

	2N1792 to 2N1804	2N1909-16 2N1805-07	2N2023-30	Units	Conditions
ON STATE					
$I_{T(RMS)}$	Max. RMS on-state current	110	110	110	A
$I_{T(AV)}$	Max. average on-state current @ Max. $T_C$ *	70*	70*	70*	A
		65*	62*	85*	°C
$I_{TSM}$	Max. peak one cycle, non-repetitive surge current	955	955	955	A
		1000*	1000*	1000*	A
		1150	1150	1150	A
		1200	1200	1200	A
$I^2t$	Max. $I^2t$ capability, for fusing	4550	4550	4550	A <sup>2</sup> s
		4150	4150	4150	A <sup>2</sup> s
$I^2t$	Max. $I^2t$ capability, for individual device fusing	6450	6450	6450	A <sup>2</sup> s
		5900	5900	5900	A <sup>2</sup> s
$I^2t$	Max. $I^2t$ capability, for individual device fusing <sup>②</sup>	64 500	64 500	64 500	A <sup>2</sup> /s
$V_{TM}$	Max. peak on-state voltage	1.85*	1.85*	1.9*	V
		2.0*	-	-	V
$I_H$	Typical holding current.	20	20	20	mA

\* JEDEC registered values.

① Units may be broken over non-repetitively without damage if di/dt does not exceed 20 A/ $\mu$ s.②  $I^2t$  for time  $t_x = I^2/t$   $\sqrt{t_x}$ .

**ELECTRICAL SPECIFICATIONS (Continued)**

	2N1792 to 2N1804	2N1909-16 2N1805-07	2N2023-30	Units	Conditions		
<b>BLOCKING</b>							
$dv/dt$	Min. critical rate-of-rise of off-state voltage	200	200	50	V/ $\mu$ s $T_J = 125^\circ\text{C}$ Exponential to 100% rated $V_{DRM}$ . Gate open circuit. $T_J = 150^\circ\text{C}$ for 2N2023-30.		
$I_{R(AV)}$ & $I_{D(AV)}$	Max. average reverse and off-state current $V_{RRM}$ & $V_{DRM}$				At rated $V_{RRM}$ , $V_{DRM}$ , $T_J = \text{max. rated}$ , gate open circuited.		
	= 25V to 150V	6.5*	6.5*	6.5*			
	= 200V	6.0*	6.5*	6.0*			
	= 250V	5.5*	5.5*	5.5*			
	= 300V	5.0*	5.0*	5.0*			
	= 400V	4.0*	4.0*	4.0*			
	= 500V to 600V	3.3* <sup>①</sup>	3.3* <sup>①</sup>	—			
	= 700V to 800V	3.0* <sup>①</sup>	3.0* <sup>①</sup>	—			
= 900V to 1200V	2.7* <sup>①</sup>	—	—				
<b>SWITCHING</b>							
$t_d$	Typical delay time	1	1	1	$\mu$ s $T_C = 25^\circ\text{C}$ , $V_{DM} = \text{rated } V_{DRM}$ , $I_{TM} = 50\text{A}$ dc resistive circuit. Gate pulse: 10V, 25 $\mu$ s source, $t_p = 6\mu$ s, $t_r = 0.1\mu$ s		
$t_r$	Typical rise time	1.5	1.5	1.5			
$t_d$	Typical turn-off time	40	40	40 (70 @ 150°C)	$\mu$ s $T_C = 125^\circ\text{C}$ , $I_{TM} = 50\text{A}$ , commutating $di/dt = -5\text{A}/\mu$ s, min. $V_R$ during turn-off interval = 50V, $dv/dt = 20\text{V}/\mu$ s linear to rated $V_{DRM}$		
$di/dt$	Max. non-repetitive rate-of-rise of turned-on current $V_{DRM}$				$\mu$ s $T_C = 125^\circ\text{C}$ , $V_{DM} = \text{rated } V_{DRM}$ $I_{TM} = (2 \times \text{rated } di/dt) \text{ A}$ Gate pulse: 20V, 15 $\mu$ s, $t_p \geq 8\mu$ s, $t_r = 0.1\mu$ s Per JEDEC Standard RS-297, 5.2.2.6.		
	= 25V to 600V	100	100	100			
	= 700V to 1200V	75	75	75			
<b>TRIGGERING</b>							
$P_{GM}$	Max. peak gate power	5*	5*	5*	W $t_p = 5\text{ms max.}$		
$P_{G(AV)}$	Max. average gate power	0.5*	0.5*	0.5*	W		
$+I_{GM}$	Max. peak positive gate current	2*	2*	2*	A		
$+V_{GM}$	Max. peak positive gate voltage	10*	10*	10*	V		
$-V_{GM}$	Max. peak negative gate voltage	5*	5*	5*	V		
$I_{GT}$	Max. required DC gate current to trigger	130* ①	130*	150* @ -85°C	mA	$T_C = -40^\circ\text{C}$ . Max. required gate trigger current is the lowest value which will trigger all units with +6V anode-to-cathode.	
		70 ①	70	70			$T_C = 25^\circ\text{C}$
		40 ①	40	—			$T_C = 125^\circ\text{C}$
		—	—	35			$T_C = 150^\circ\text{C}$
		35	35	35			$T_C = 25^\circ\text{C}$ +6V anode-to-cathode

\*JEDEC registered values.

①  $V_{RRM}$  20% greater than  $V_{DRM}$ .

① For 2N1803, 1804:  $I_{GT} = 200\text{mA} @ -40^\circ\text{C}$ ; 110mA @  $25^\circ\text{C}$ ; 60 mA @  $125^\circ\text{C}$ .

**ELECTRICAL SPECIFICATIONS (Continued)**

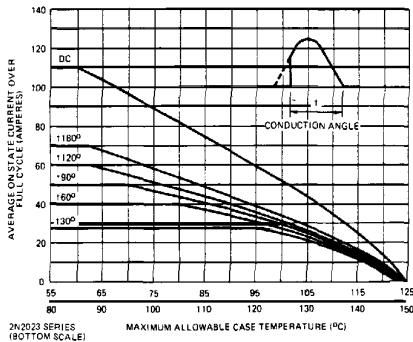
	2N1792 to 2N1804	2N1809-16 to 2N1805-07	2N2023-30	Units	Conditions
TRIGGERING (Cont.)					
V <sub>GT</sub>	Max. required DC gate voltage to trigger	—	—	3*	V T <sub>C</sub> = -65°C. Max. required gate trigger voltage is the lowest value which will trigger all units with +6V anode-to-cathode. T <sub>C</sub> = -40°C T <sub>C</sub> = 25°C T <sub>C</sub> = 25°C +6V anode-to-cathode
		3*	3*	—	
		2.5	2.5	2.0	
	Typical DC gate voltage to trigger	1.2	1.2	1.2	
V <sub>GD</sub>	Max. DC gate voltage not to trigger	0.25*	0.25*	0.25* @ 150°C	V T <sub>C</sub> = 125°C. Max. gate voltage not to trigger is the maximum value which will not trigger any unit with rated V <sub>DRM</sub> anode to cathode.

**THERMAL-MECHANICAL SPECIFICATIONS**

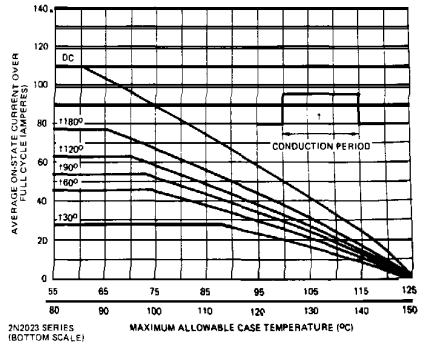
T <sub>J</sub>	Operating junction temperature range	-65° to 125*	-40° to 125*	-65° to 150*	°C	
T <sub>stg</sub>	Storage temperature range	-40° to 150*	-40° to 125*	-65° to 150*	°C	
R <sub>thJC</sub>	Max. internal thermal resistance, junction-to-case	0.4* ①	0.4*	0.4*	deg. C/W	DC operation
R <sub>thCS</sub>	Thermal resistance, case-to-sink	0.1	0.1	0.1	deg. C/W	Mounting surface smooth, flat and greased.
T	Mounting torque				N·m	Non-lubricated threads
	Min.	14.5 (1.25)			(lb·ft·in)	
	Max.	17 (150)				
	Max. torque on screw in flagterminal	1.4 (12)	—	—	N·m (lb·ft·in)	Non-lubricated threads TO-20BAD (TO-83) only
wt	Approximate weight	100 (3.5)			g (oz)	
	Case style	2N1805-07; 2N1809-16; 2N2023-30; TO-209AC (TO-94) 1A-13)			JEDEC	
		2N1792-1804; TO-20BAD (TO-83) 1A-14)			JEDEC	

\*JEDEC registered values.

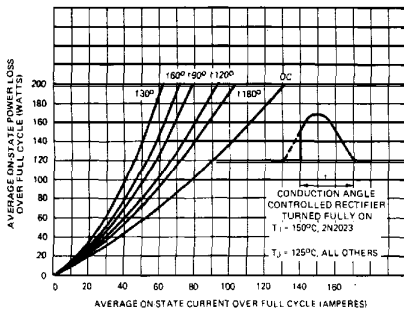
① 2N1803, 2N1804: R<sub>thJC</sub> = 0.35 deg. C/W.



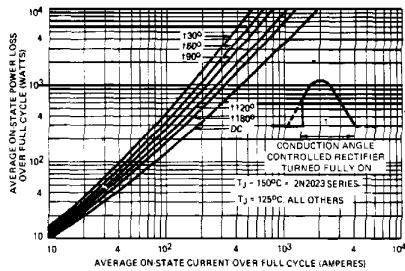
**Fig. 1 — On-State Current Vs. Case Temperature (Sinusoidal Current Waveform, 50 to 400 Hz)**



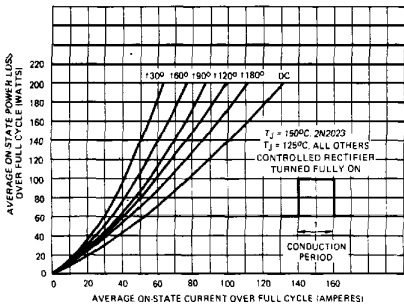
**Fig. 2 — On-State Current Vs. Case Temperature (Rectangular Current Waveform, 50 to 400 Hz)**



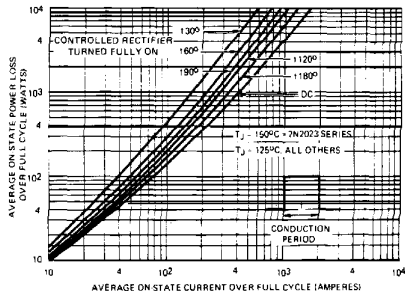
**Fig. 3 – Maximum Low-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)**



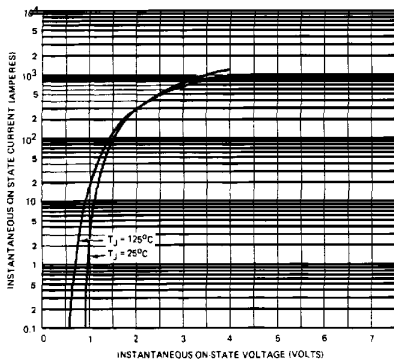
**Fig. 4 – Maximum High-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)**



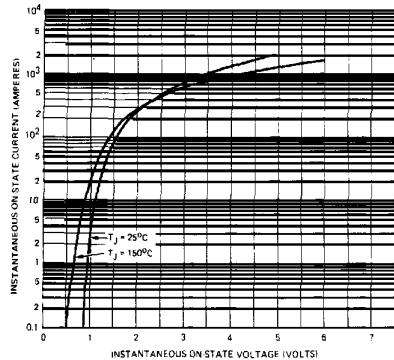
**Fig. 5 – Maximum Low-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)**



**Fig. 6 – Maximum High-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)**



**Fig. 7 – Maximum Instantaneous On-State Voltage Vs. Current (2N1792, 2N1805 and 2N1909 Series)**



**Fig. 8 – Maximum Instantaneous On-State Voltage Vs. Current (2N2023 Series)**

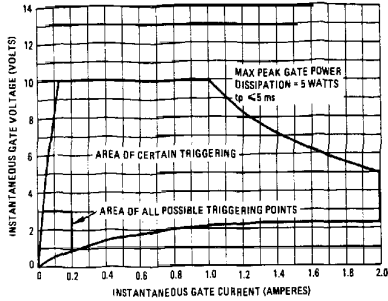


Fig. 9 - Gate Characteristics

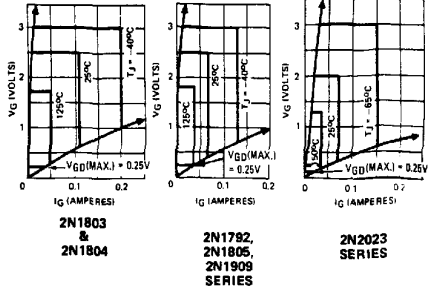


Fig. 9A - Areas of All Possible Triggering Points Vs. Junction Temperature

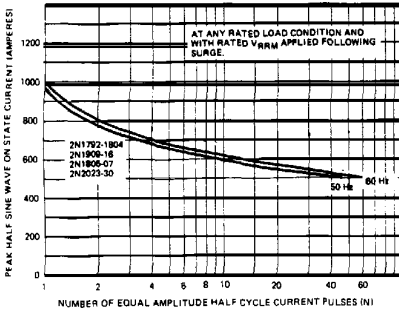


Fig. 10 - Maximum Non-Repetitive Surge Current Vs. Number of Current Pulses

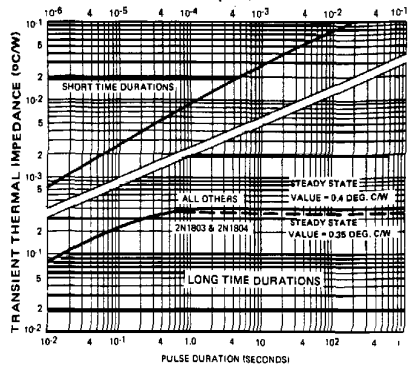
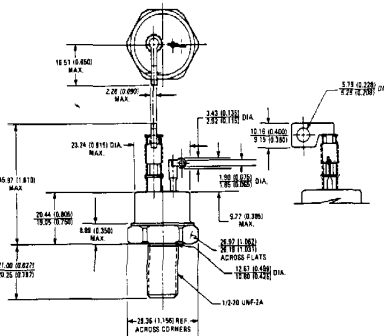


Fig. 11 - Transient Thermal Impedance, Junction to Case, Vs. Pulse Duration



IR Case Style A-14  
 Conforms to JEDEC Outline TO-208AD (TO-83)  
 All Dimensions in Millimeters and (Inches)