

PowerMOS transistor

BUK443-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

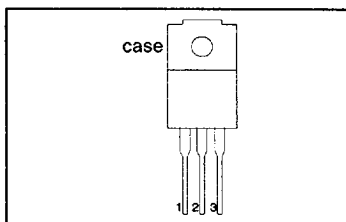
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK443	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	9	8	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

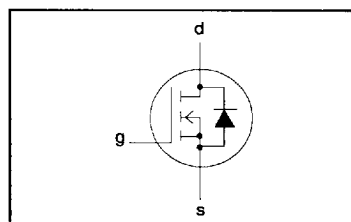
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-100A	-100B	
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
I_D	Drain current (DC)	$T_{hs} = 25 \text{ }^\circ\text{C}$	-	9	8	A
I_D	Drain current (DC)	$T_{hs} = 100 \text{ }^\circ\text{C}$	-	5.7	5	A
I_{DM}	Drain current (pulse peak value)	$T_{hs} = 25 \text{ }^\circ\text{C}$	-	36	32	A
P_{tot}	Total power dissipation	$T_{hs} = 25 \text{ }^\circ\text{C}$	-	25		W
T_{stg}	Storage temperature	-	-55	150		$^\circ\text{C}$
T_j	Junction Temperature	-	-	150		$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-hs)}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient		-	55	-	K/W

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STATIC CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_J = 25\text{ }^{\circ}\text{C}$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_J = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	-	0.15	0.16	Ω
		BUK443-100A	-	0.17	0.2	Ω
		BUK443-100B	-			

DYNAMIC CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5\text{ A}$	4.0	5.5	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 2.9\text{ A};$	-	10	20	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$	-	25	40	ns
t_{doff}	Turn-off delay time	$R_{gen} = 50\text{ }\Omega$	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION

 $T_{hs} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. $\leq 65\%$; clean and dustfree	-	-	1500	V
C_{isol}	Capacitance from T2 to external heatsink	$f = 1\text{ MHz}$	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	$I_F = 9\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	1.3	V
t_{rr}	Reverse recovery time	$I_F = 9\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	80	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	0.5	-	μC

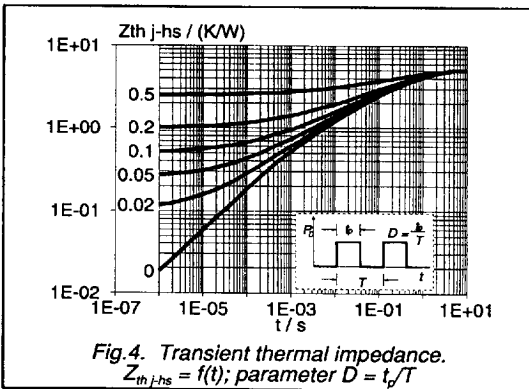
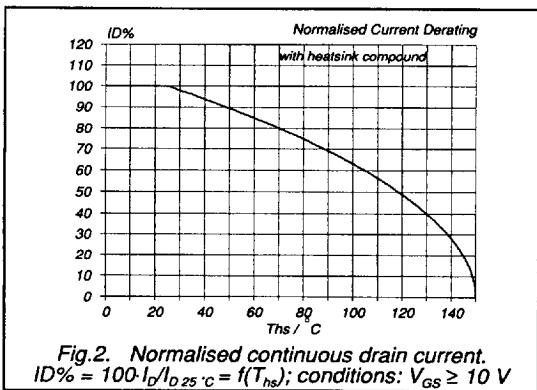
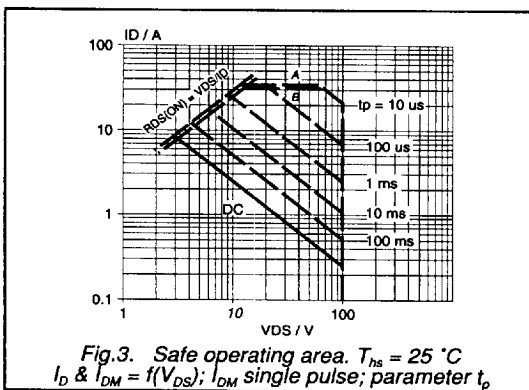
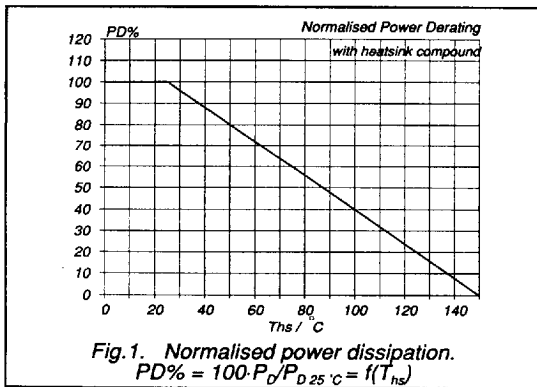
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AVALANCHE LIMITING VALUE

$T_{hs} = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 14\text{ A}$; $V_{DD} \leq 50\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$	-	-	70	mJ



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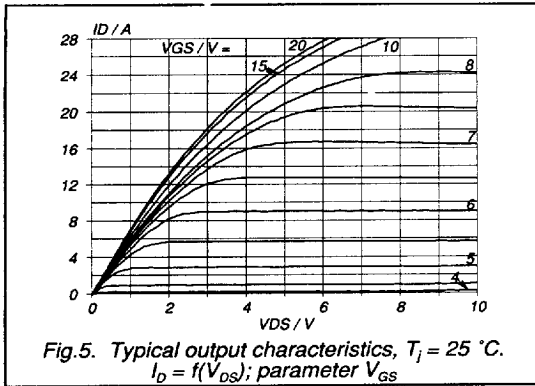


Fig. 5. Typical output characteristics, $T_j = 25\text{ }^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

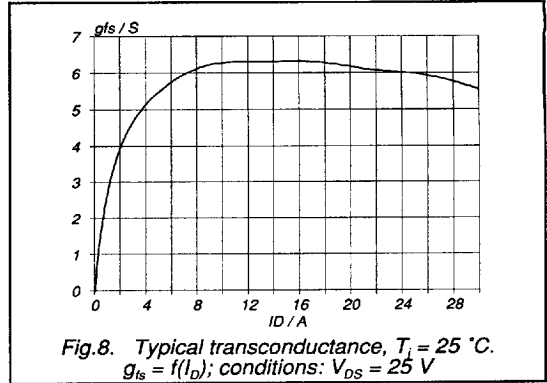


Fig. 8. Typical transconductance, $T_j = 25\text{ }^\circ\text{C}$.
 $g_s = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

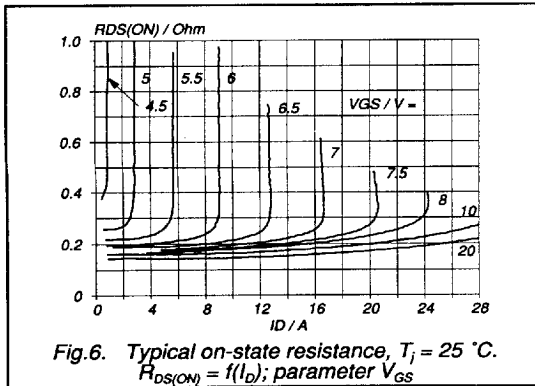


Fig. 6. Typical on-state resistance, $T_j = 25\text{ }^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

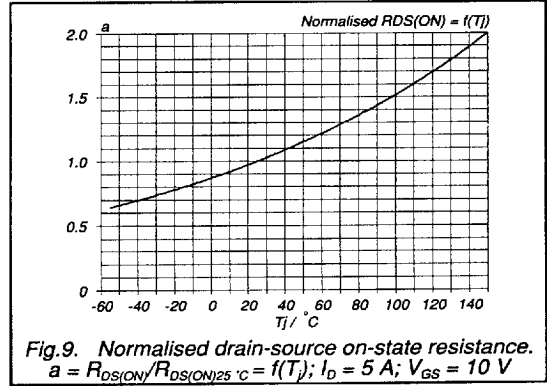


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^\circ\text{C}} = f(T_j)$; $I_D = 5\text{ A}$; $V_{GS} = 10\text{ V}$

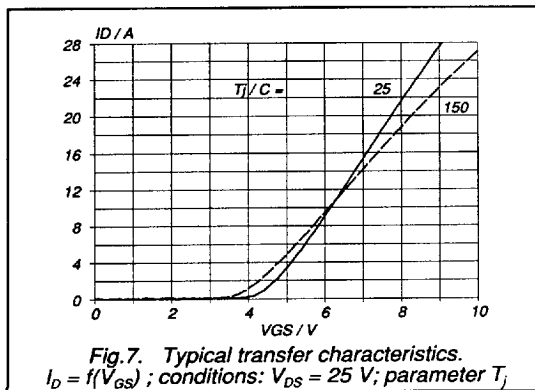


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

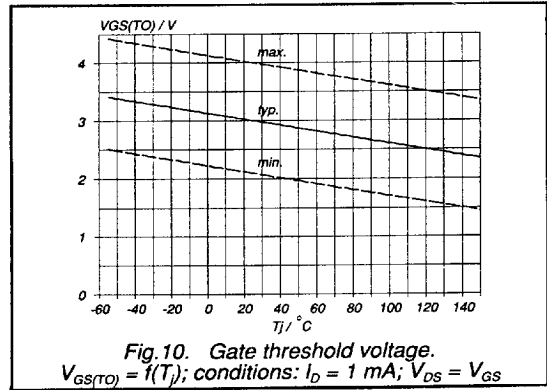


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

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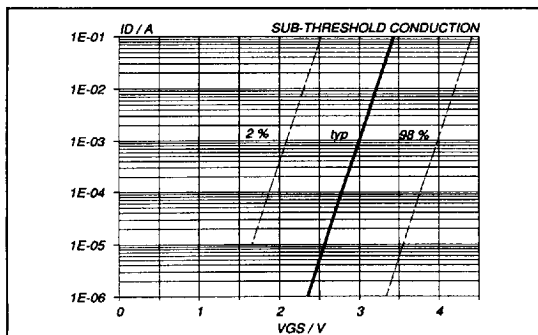


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

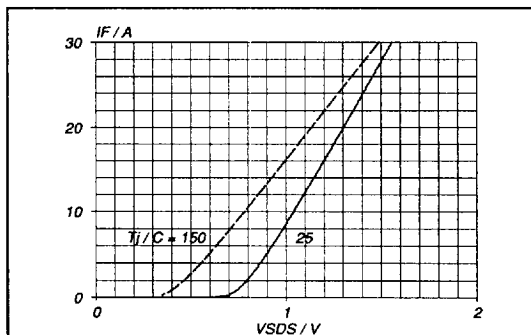


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

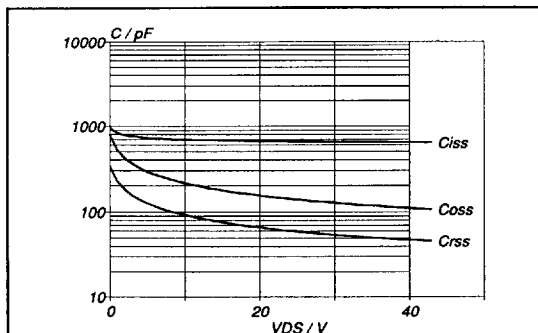


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

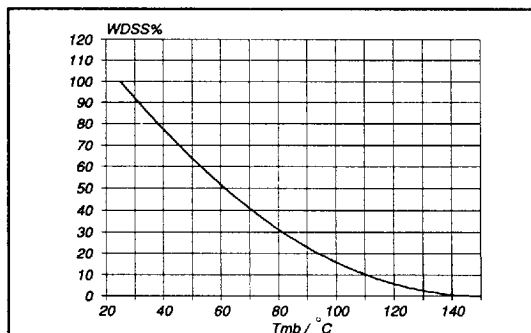


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14\text{ A}$

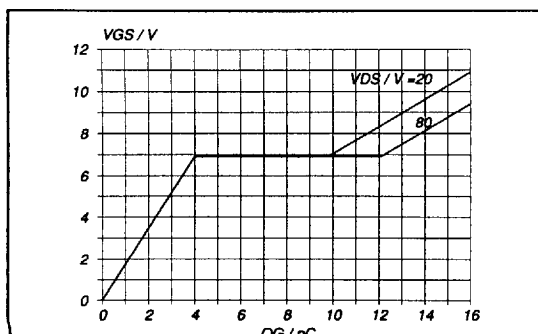


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 14\text{ A}$; parameter V_{DS}

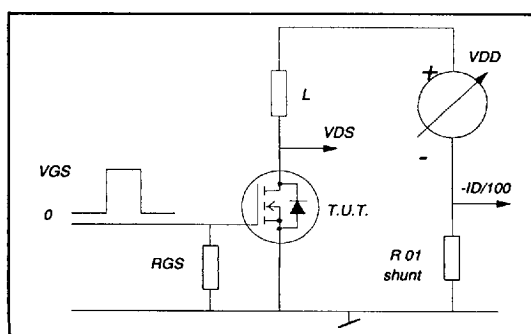


Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$