

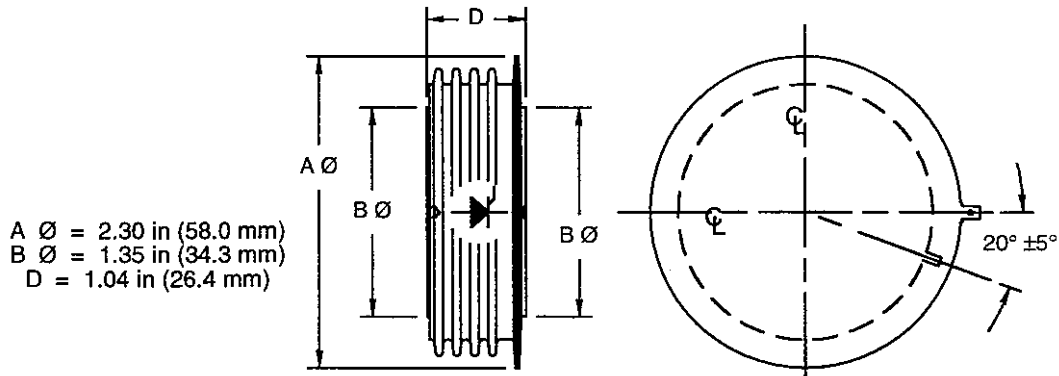
The C602 is specifically designed for phase control applications and is processed by multidiffusion, utilizing 40mm diameter silicon and a unique pilot gate. It is supplied in a disk package ready to mount using commercially available heat dissipators and mechanical clamping hardware.

**MAXIMUM ALLOWABLE RATINGS**

TYPE	$V_{DRM}/V_{RRM}^1$ REPETITIVE $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	$V_{DRM}/V_{RRM}^1$ REPETITIVE $T_J = 0^\circ\text{C to } +125^\circ\text{C}$	TRANSIENT PEAK REVERSE VOLTAGE (NON-RECURRENT < 5 MILLISECONDS) $V_{RSM}$ $T_J = -40^\circ\text{C to } +125^\circ\text{C}$
C602PS	1700 Volts	1800 Volts	1800 Volts
C602PN	1800	1900	1900
C602PT	1900	2000	2000
C602L	2000	2100	2100
C602LA	2100	2200	2200
C602LB	2200	2300	2300
C602LC	2300	2400	2400
C602LD	2400	2500	2500
C602LE	2500	2600	2600
C602LM	2600	2700	2700

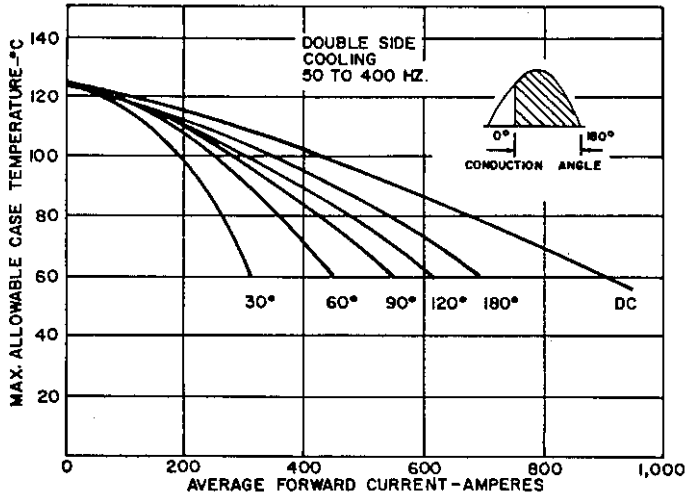
Consult factory for higher voltage grades.

- Average Forward Current, On-State . . . . . Depends on Conduction Angle
- Peak One-Cycle Surge On-State Current,  $I_{TSM}$  . . . . . 10,000 Amperes
- Maximum Rate-of-Rise of Anode Current Turn-On Interval  
 (Switching Rates  $\leq 400$  Hz) . . . . . Switch From < 600V, 75A/ $\mu\text{sec}$   
 (See Curve 9. for Recommended Load Line). . . . . Switch From < 1000V, 50A/ $\mu\text{sec}$   
 . . . . . Switch From < 1500V, 35A/ $\mu\text{sec}$
- $I^2t$  (for fusing) (at 8.3 milliseconds) . . . . . 415,000 Ampere<sup>2</sup> Seconds
- Peak Gate Power Dissipation,  $P_{GM}$  . . . . . 40 Watts
- Average Gate Power Dissipation,  $P_{G(AV)}$  . . . . . 5 Watts
- Peak Reverse Gate Voltage,  $V_{GRM}$  . . . . . 5 Volts
- Storage and Operating Temperatures,  $T_{STG}$  and  $T_J$  . . . . . Refer Above
- Mounting Force Required . . . . . 4000 Lbs.  $\pm 10\%$   
 17.8 KN  $\pm 10\%$

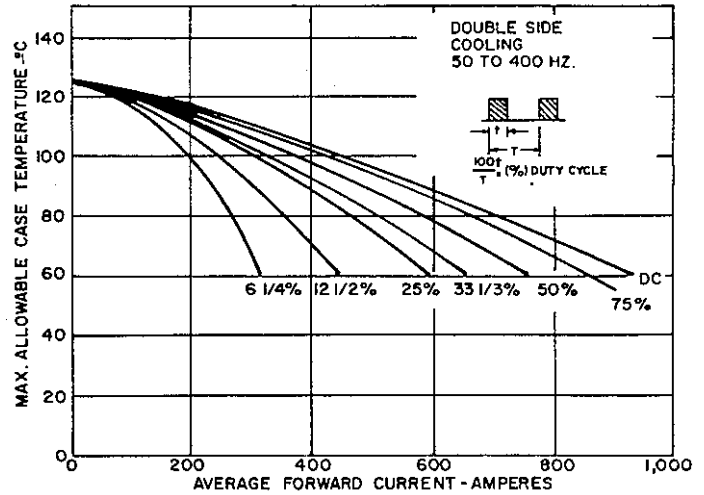


## CHARACTERISTICS

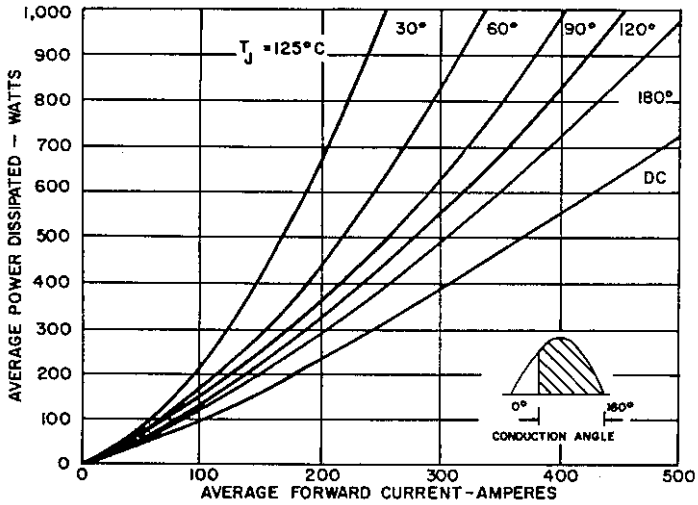
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and Forward Blocking Current	$I_{DRM}$ and $I_{RRM}$	—	10	15	mA	$T_J = +25^\circ\text{C}$ , $V = V_{DRM} = V_{RRM}$
Peak Reverse and On-State Blocking Current	$I_{DRM}$ and $I_{RRM}$	—	15	35	mA	$T_J = +125^\circ\text{C}$ , $V = V_{DRM} = V_{RRM}$
Effective Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	—	—	.036	$^\circ\text{C}/\text{Watt}$	Junction-to-Case, Double-Side Cooled (DC)
Critical Exponential Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	$dv/dt$	500	—	—	$\text{V}/\mu\text{sec}$	$T_J = +125^\circ\text{C}$ , $V_{DRM} = .67$ Rated, Gate Open.
Holding Current	$I_H$	—	100	250	mAdc	$T_C = +25^\circ\text{C}$ , Anode Supply = 20 Vdc. Initial Forward Current = 500 Amps.
Latching Current	$I_L$	—	—	1	Adc	$T_C = +25^\circ\text{C}$ , Anode Voltage = 24 Vdc. Load Resistance 12 Ohms Max.
Delay Time	$t_d$	—	1.8	—	$\mu\text{sec}$	Switching From 900 Volts, 20V/10 $\Omega$ , .5 $\mu\text{sec}$ Rise Time
Gate Pulse Width Necessary to Trigger		—	—	10	$\mu\text{sec}$	See Figure 9.
Gate Trigger Current	$I_{GT}$	—	80	150	mAdc	$T_C = 25^\circ\text{C}$ , $V_D = 10$ Vdc, $R_L = 3$ Ohms
		5.0	15	75		$T_C = +125^\circ\text{C}$ , $V_D = .5$ x Rated, $R_L = 1000$ Ohms
Gate Trigger Voltage	$V_{GT}$	—	2.6	4.5	Vdc	$T_C = 0^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_D = 10$ Vdc, $R_L = 3$ Ohms
		.2	—	—		$T_C = 125^\circ\text{C}$ , $V_D = .5$ x Rated, $R_L = 1000$ Ohms
Peak On-State Voltage	$V_{TM}$	—	—	1.90	Volts	$T_C = +125^\circ\text{C}$ , $I_T = 1000$ Amps. Peak, Duty Cycle $\leq 0.01\%$
Circuit Commutated Turn-Off Time	$t_q$	—	125	250	$\mu\text{sec}$	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 450$ Amps. (3) $V_R = 75$ Volts Min. (4) 50% $V_{DRM}$ Reapplied (5) Rate-of-rise of Reapplied Forward Blocking Voltage = .25V/ $\mu\text{sec}$ . Linear (6) Gate Bias = Open During Turn-Off Interval (7) Duty Cycle $\leq 0.01\%$
Suppressible Surge Current	$I_{TM(SUP)}$	—	7500	—	Amps	(1) $T_C = 115^\circ\text{C}$ (2) $V_R = .67 V_{RRM}$ (3) .67 $V_{DRM}$ , Applied 8.3 msec. After Completion of Surge (4) Figure 13.



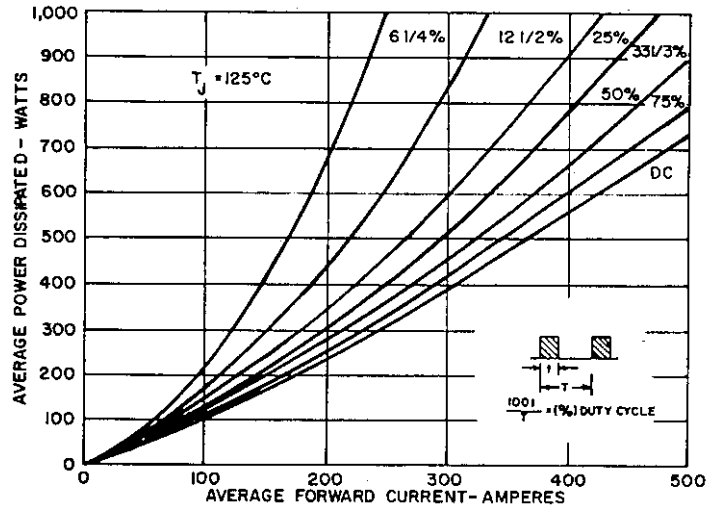
**1. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM (DOUBLE-SIDE COOLED)**



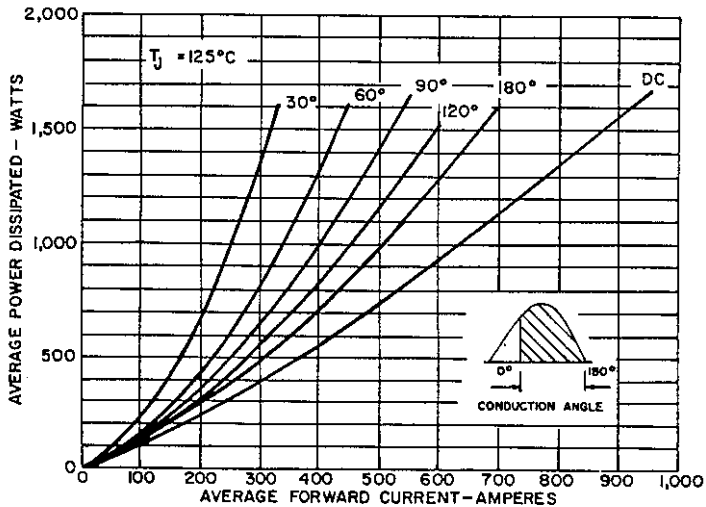
**2. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM (DOUBLE-SIDE COOLED)**



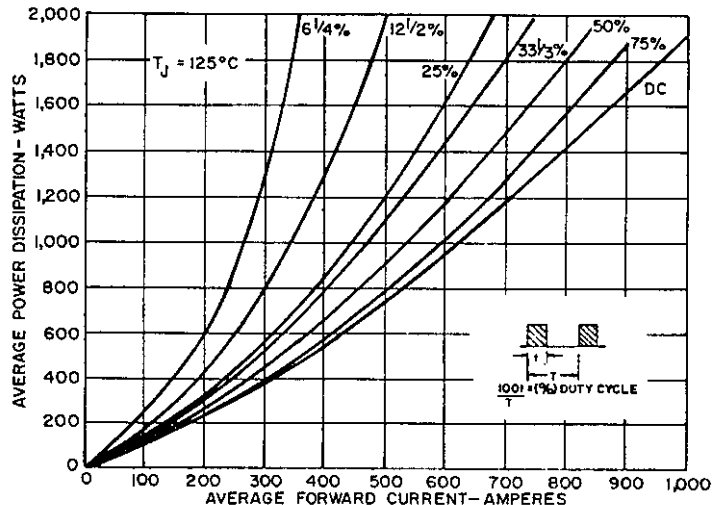
**3. AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM**



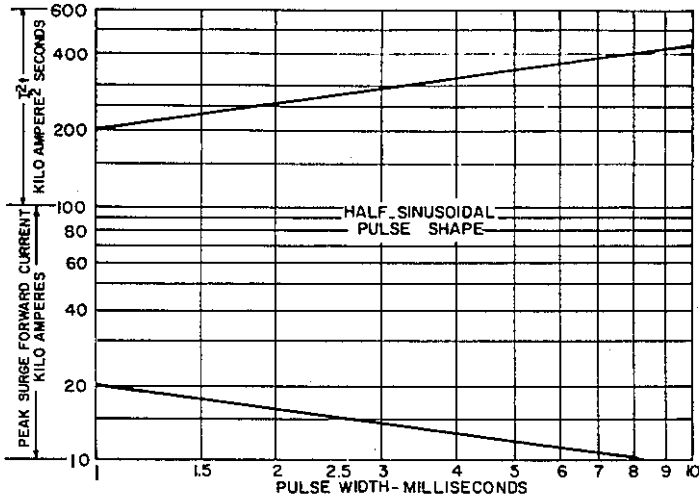
**4. AVERAGE FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM**



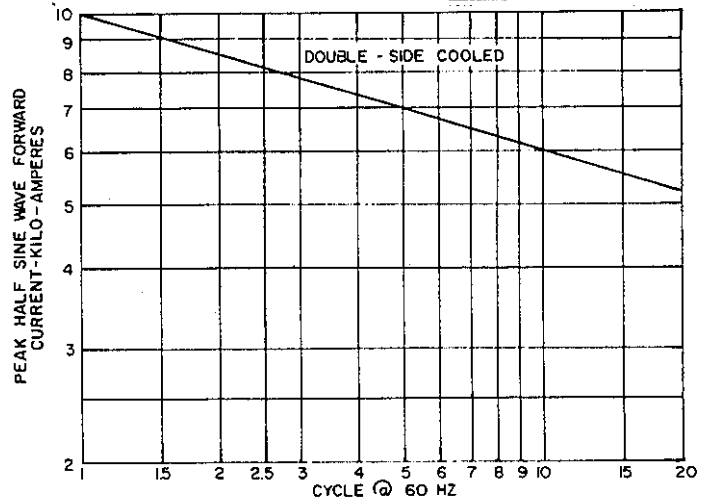
**5. EXTENDED FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM**



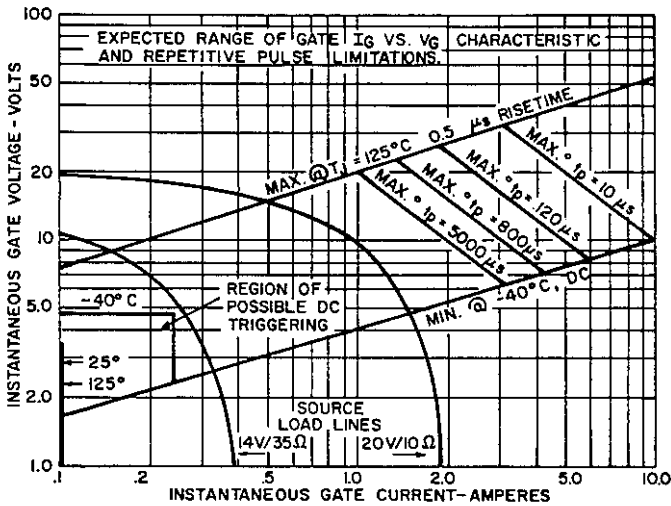
**6. EXTENDED FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM**



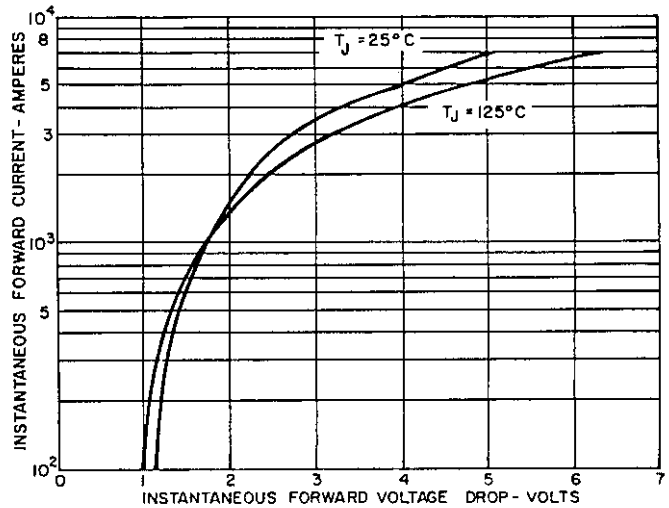
7. SUB CYCLE SURGE AND  $I^2t$  RATING FOLLOWING RATED LOAD CONDITIONS



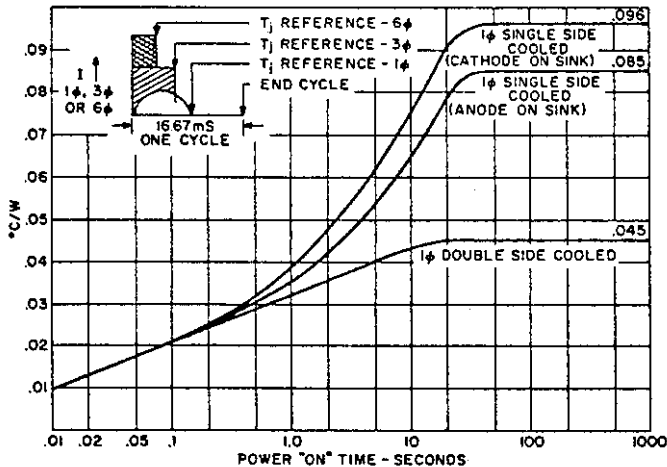
8. MAXIMUM ALLOWABLE SURGE CURRENT FOLLOWING RATED LOAD CONDITIONS



9. GATE TRIGGERING CHARACTERISTICS



10. FORWARD CONDUCTION CHARACTERISTIC, ON-STATE



11. TRANSIENT THERMAL IMPEDANCE - JUNCTION-TO-CASE

NOTES:

- For 3φ thermal resistance add .0037°C/W along entire curve length.
- For 6φ thermal resistance add .001°C/W along entire curve length.
- For DC thermal resistance subtract .005°C/W along entire curve length.