CY7C167A

16K x 1 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns**
- **Low active power**
  - **— 495 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C167A is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

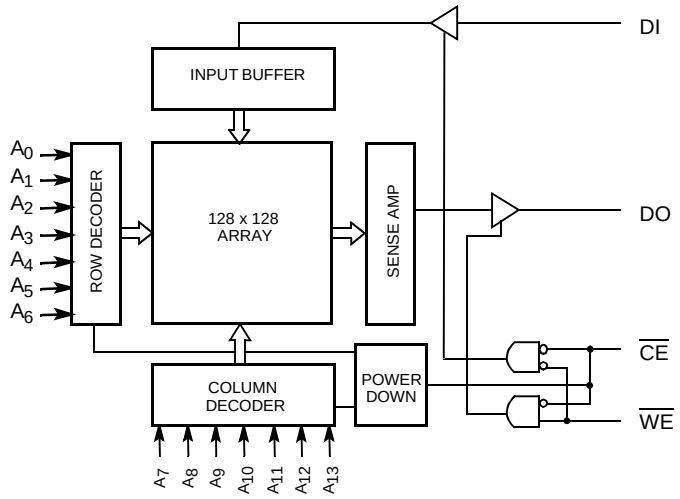
Writing to the device is accomplished when the Chip Select ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the Chip Enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when Chip Enable is HIGH, or Write Enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



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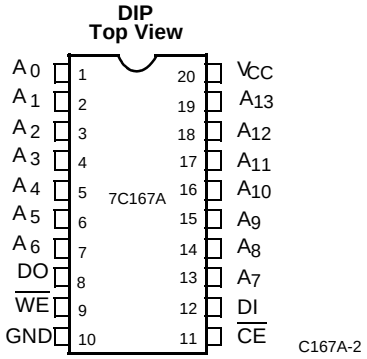
Pin Configuration



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Selection Guide

	7C167A-15	7C167A-20	7C167A-25	7C167A-35	7C167A-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	90	90	90	90	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage..... –3.0V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C167A-15		7C167A-20		7C167A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[2]		–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled	–10	+10	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		90		90		90	mA
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		40		40		20	mA

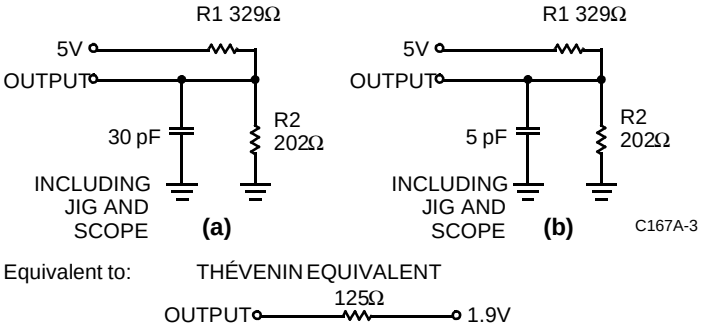
Parameter	Description	Test Conditions	7C167A-35		7C167A-45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[2]		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		90		90	mA
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		20		20	mA

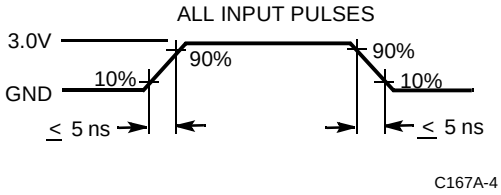
Notes:
1. T_A is the case temperature.
2. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF
C_{CE}	Chip Enable Capacitance		6	pF

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[6]

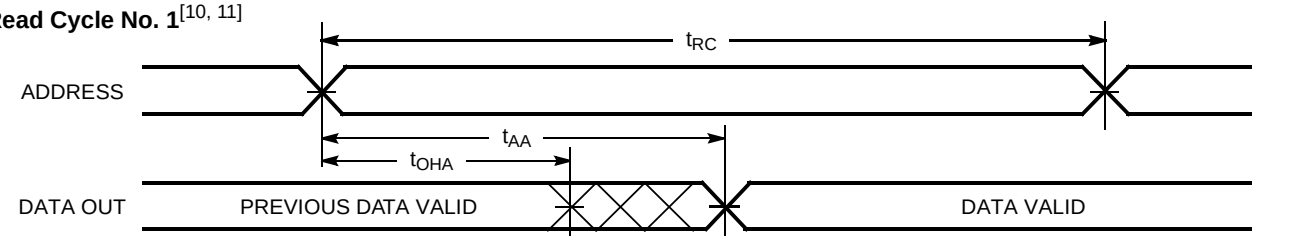
Parameter	Description	7C167A-15		7C167A-20		7C167A-25		7C167A-35		7C167A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		30				ns
t_{AA}	Address to Data Valid		15		20		25		30			ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		5		5		5		ns

Notes:

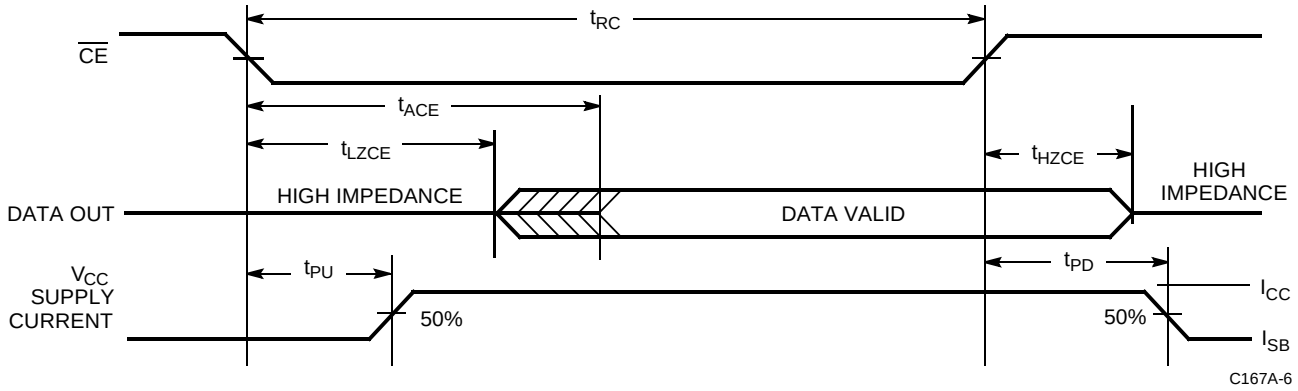
5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
8. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

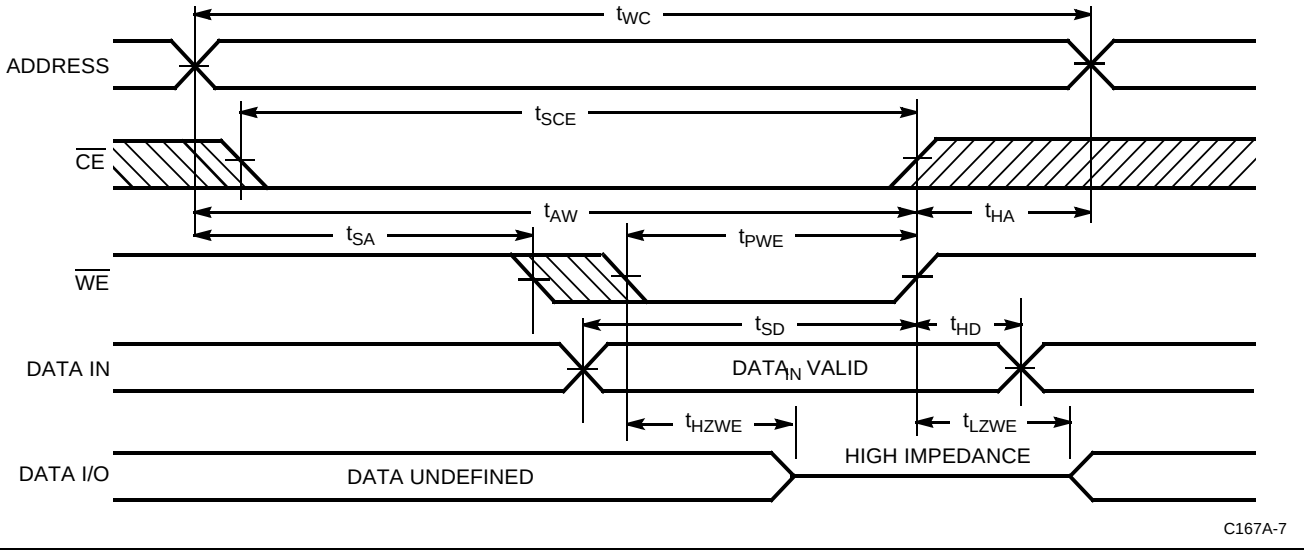
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



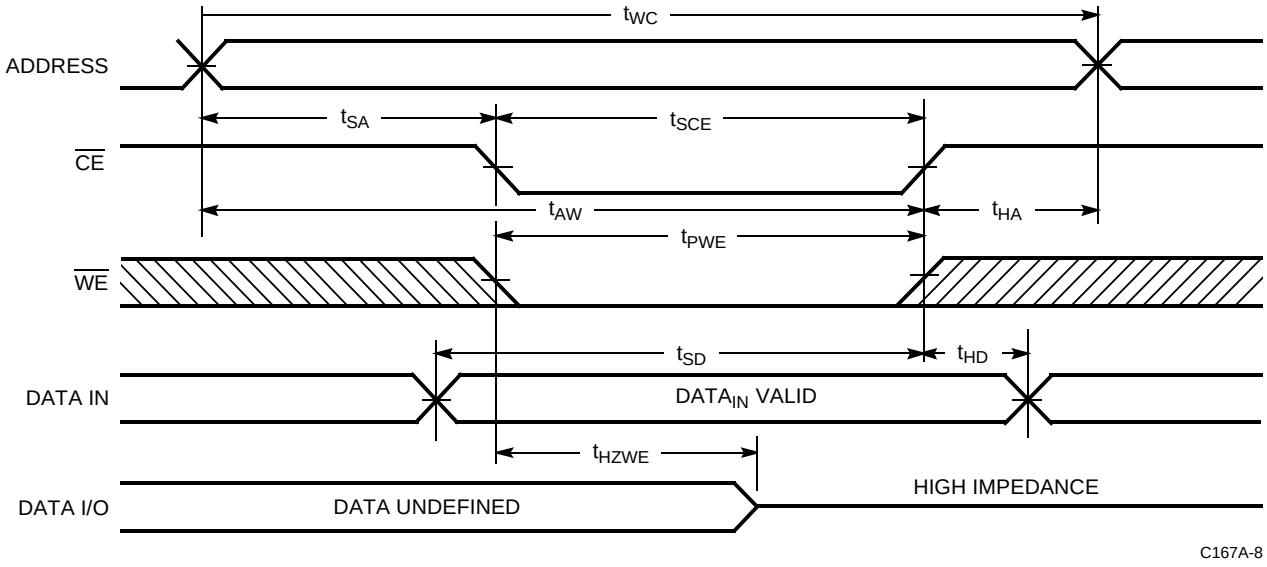
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9]



Notes:
10. $\overline{WE}$ is high for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13]



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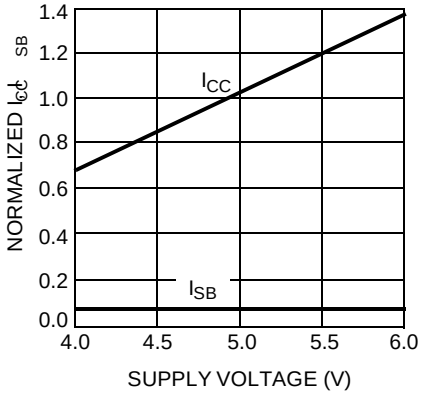
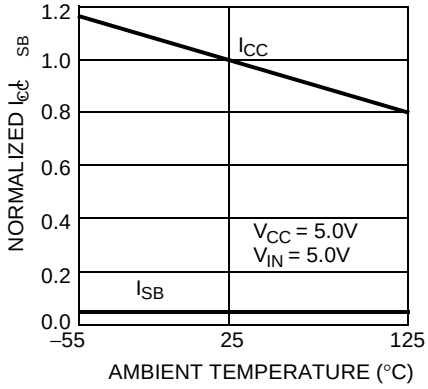
Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

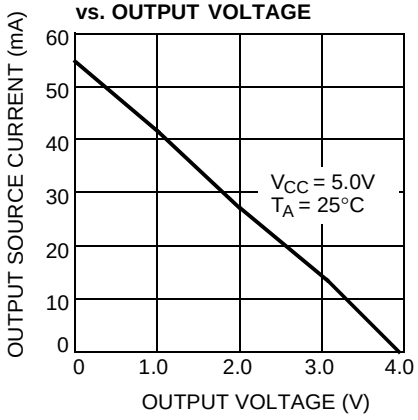
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



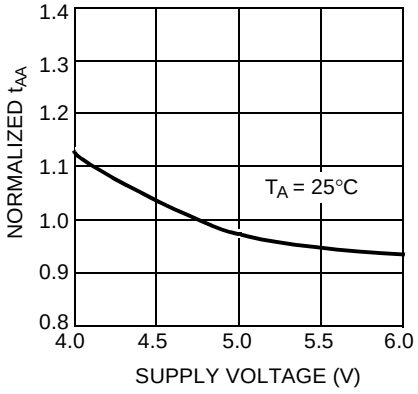
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



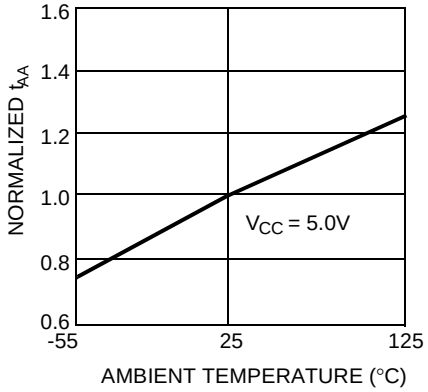
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



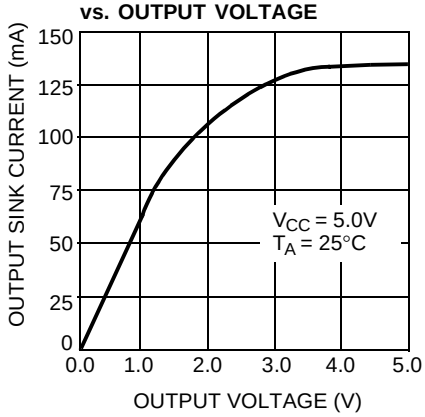
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



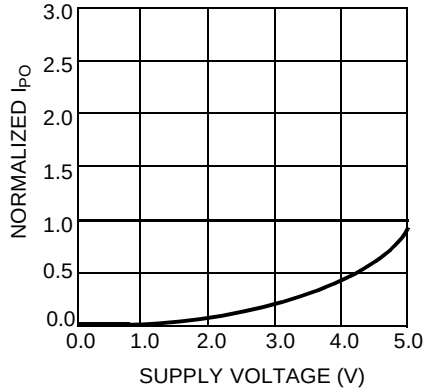
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



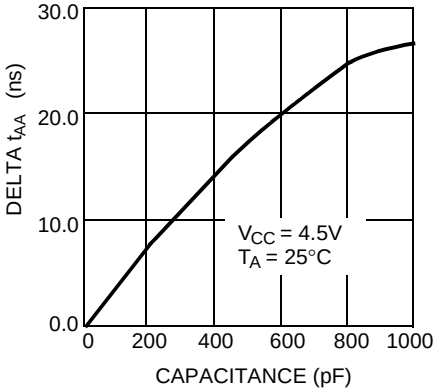
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



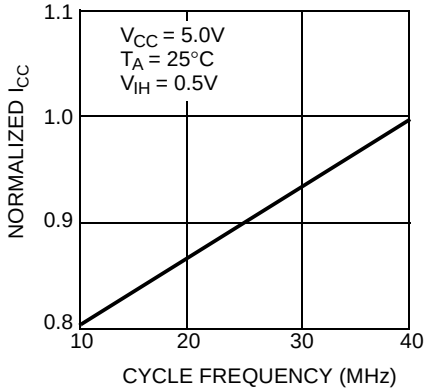
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME

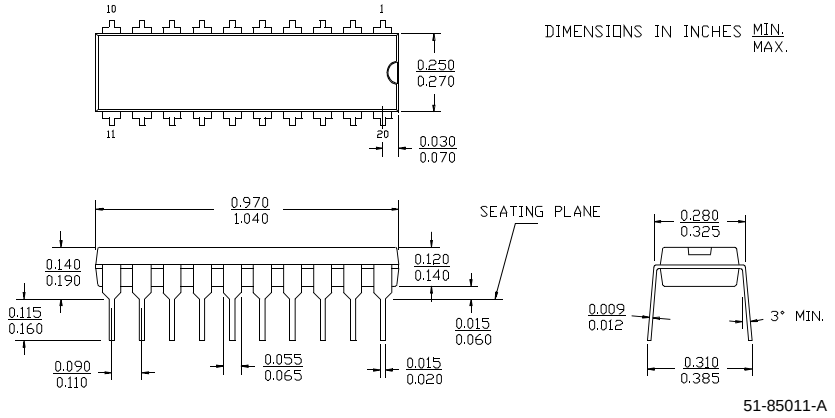


Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	80	CY7C167A-15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-15VC	V5	20-Lead Molded SOJ	
20	80	CY7C167A-20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-20VC	V5	20-Lead Molded SOJ	
25	60	CY7C167A-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-25VC	V5	20-Lead Molded SOJ	
35	60	CY7C167A-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-35VC	V5	20-Lead Molded SOJ	
45	50	CY7C167A-45PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C167A-45VC	V5	20-Lead Molded SOJ	

Package Diagrams

20-Lead (300-Mil) Molded DIP P5



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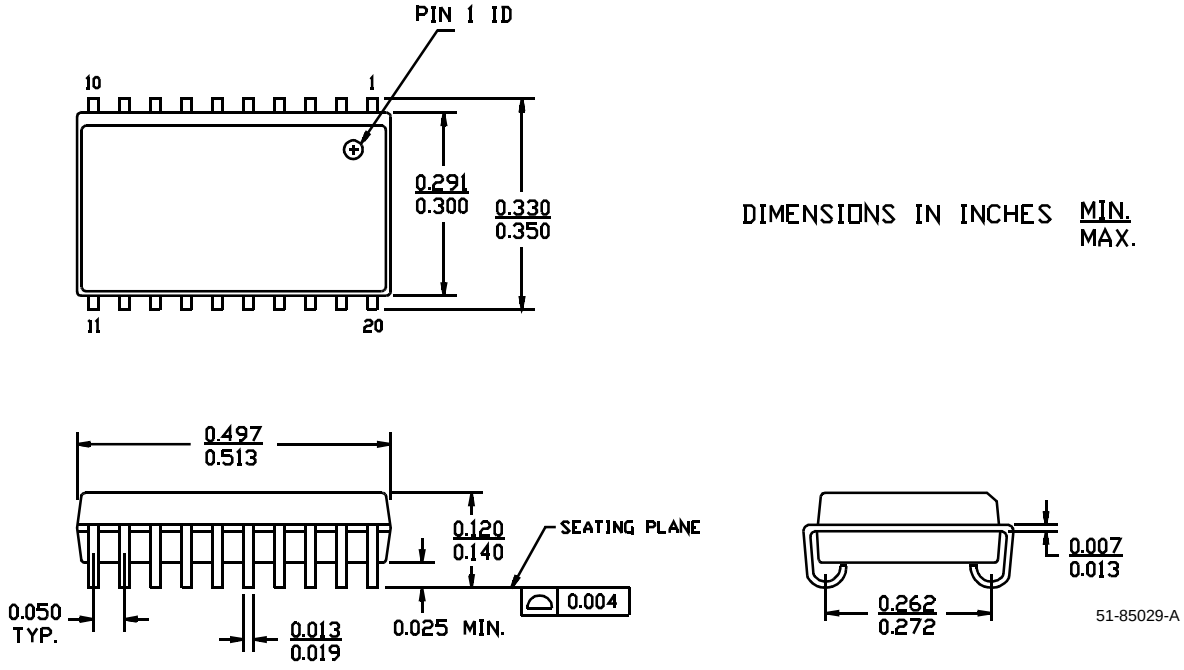
20-Lead (300-Mil) Molded SOJ V5



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Document Title: CY7C167A 16K x 1 Static RAM Document Number: 38-05027				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106813	09/10/01	SZV	Change from Spec number: 38-00093 to 38-05027