

# FUJI Power Supply Control IC

General PWM-IC

# FA5604/5605/5606

# *Application Note*

April-2011  
Fuji Electric Co.,Ltd.

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**Note**

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- Parts tolerance and characteristics are not defined in all application described in this Date book. When design an actual circuit for a product, you must determine parts tolerance and characteristics for safe and economical operation.

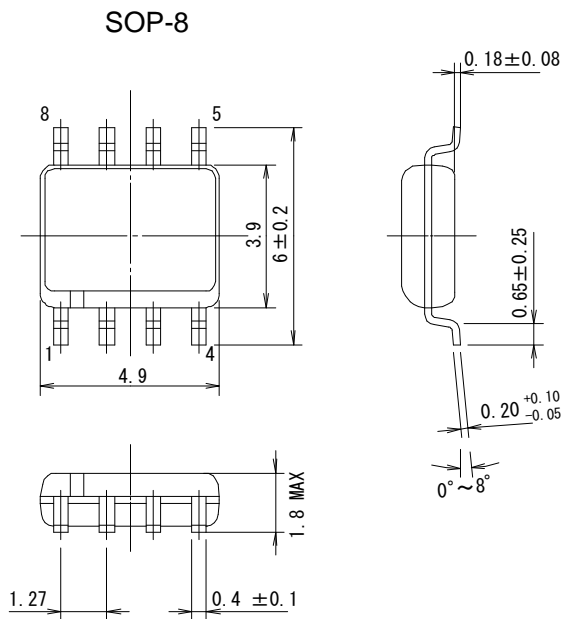
### 1. Description

The FA5604/05/06 is the PWM type switching power supply control IC that can directly drive power MOSFET. This IC realizes the low power consumption with reducing the switching frequency at light load. This IC contains many functions in a small 8-pin package. With this IC, a high-performance and compact power supply can be created because not many external discrete components are needed.

### 2. Features

- Voltage mode control
- Systems organized by circuit methods
  - FA5604: Applied to forward power supplies (maximum duty cycle = 46%)
  - FA5605/FA5606: Applied to flyback power supplies (maximum duty cycle = 70%)
- Automatically reduces the switching frequency to suppress loss in stand-by mode
- The switching frequency can be set (RT pin)
- A drive circuit for connecting a power MOSFET directly
- Output peak current: +1.0A / -0.5A
- Overcurrent of primary side limiting function (IS pin negative voltage sense)
- Overload protection function (switching frequency control by VF pin)
- Overload protection function (CS pin)
- Built-in output overvoltage latch protection (stopping the latch by pulling up the CS terminal by external signals)
- Undervoltage lockout function (17.5V ON / 9.7V OFF)
- 8-pin package (SOP-8)

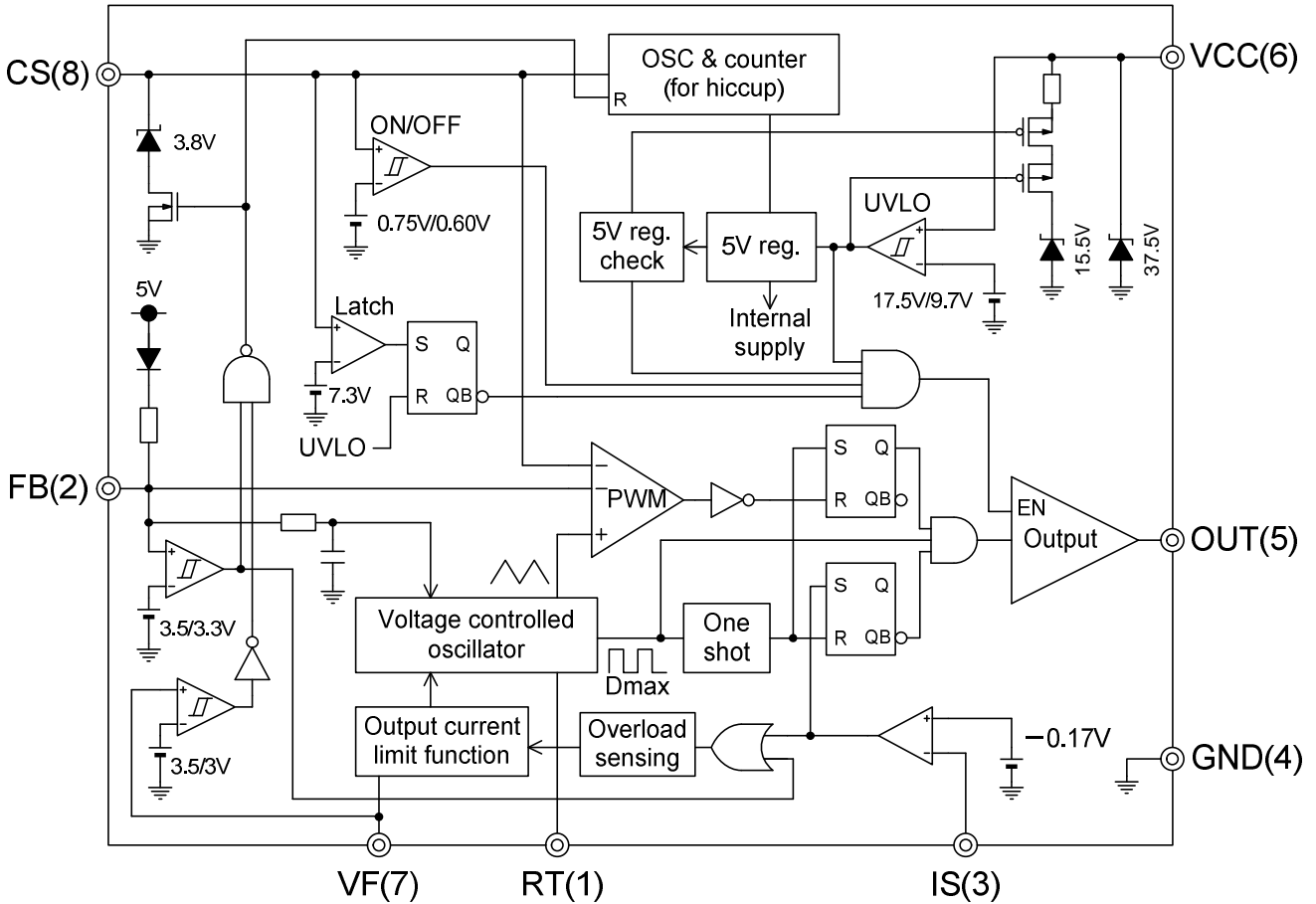
### 3. Outline



### 4. Types of FA5604

| type    | Max. duty cycle(typ) | Frequency reduction mode at light-load | Hiccup operation at overload                | Overcurrent detection | Package |
|---------|----------------------|--|---|-----------------------|---------|
| FA5604N | 46%                  | FB voltage:<br>1.8 V/1.95 V            | Operation period:<br>shutdown period = 1:7  | - detection           | SOP-8   |
| FA5605N | 70%                  |  | Operation period:<br>shutdown period = 1:15 |                       |         |
| FA5606N |                      | FB voltage:<br>1.55 V/1.65 V           | Operation period:<br>shutdown period = 1:7  |                       |         |

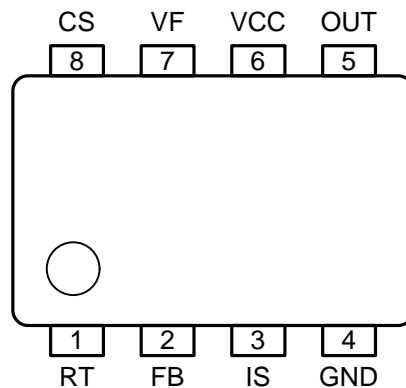
5. Block diagram



6. Pin assignment

| Pin | Symbol | Function                                 | Description   |
|-----|--------|--|---|
| 1   | RT     | Oscillator timing resistor               | Connected to oscillator timing resistor                                     |
| 2   | FB     | Feedback                                 | Input of PWM comparator OLP   |
| 3   | IS     | Overcurrent detection                    | Input of the overcurrent limiting function (-)                              |
| 4   | GND    | Ground                                   | Signal ground of the power IC   |
| 5   | OUT    | Output                                   | Output for driving a power MOSFET   |
| 6   | VCC    | Power supply                             | Power supply  |
| 7   | VF     | Switching Frequency Control at over load | Overload protection   |
| 8   | CS     | Soft-start and ON/OFF control            | Soft-start, ON/OFF function, OLP-hiccup, and latch-mode shutdown operations |

Note) Power ground PGND (▼) and signal ground GND (▽) are connected through current sensing resistor Rs.



## 7. Rating and Characteristics

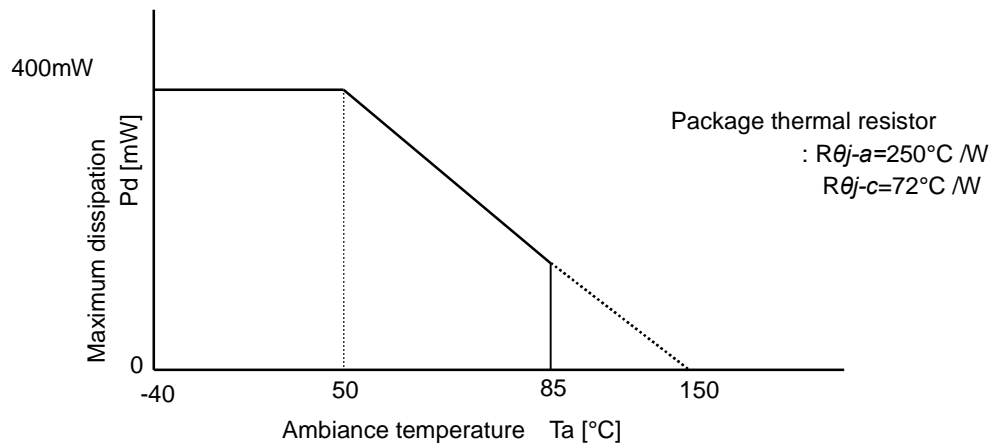
The contents are subject to change without notice for specification changes or other reasons.  
 Current characteristics; “+” is sink current and “-” is source current

### (1) Absolute maximum ratings

| Item                                      | Symbol | Rating          | Unit |
|---|--------|-----------------|------|
| Supply Voltage                            | VCC    | 35              | V    |
| Supply Current                            | ICC    | 30              | mA   |
| Peak current at OUT pin                   | IOH    | - 0.5           | A    |
|   | IOL    | +1.0            | A    |
| Voltage at OUT pin                        | VOUT   | -0.3 to VCC+0.3 | V    |
| Input voltage at VF pin                   | VVF    | -0.3 to VCC+0.3 | V    |
| Input current at CS pin                   | VCS    | 2.0             | mA   |
| Input voltage at FB,IS pin                | VLT    | - 0.3 to 5.0    | V    |
| Power dissipation (Ta<50°C)               | Pd     | 400             | mW   |
| Maximum junction temperature in operation | Tj     | - 40 to +150    | °C   |
| Storage temperature                       | Tstg   | -40 to +150     | °C   |

Note) There are cases where the IC cannot output the rating current depending on VCC voltage or temperature.

※Maximum dissipation curve



### (2) Recommended Operating Conditions

| Item                              | Symbol | MIN | TYP | MAX | Unit |
|-----------------------------------|--------|-----|-----|-----|------|
| Supply voltage                    | VCC    | 11  | 18  | 30  | V    |
| VCC pin capacitance               | CVCC   | 10  | 47  | 220 | μF   |
| Switching frequency (FB>VthFBS2)  | Fosc   | 100 | 190 | 300 | kHz  |
| Timing resistance                 | Rt     | 7.5 | 12  | 24  | kΩ   |
| Ambiance temperature in operation | Ta     | -40 |     | +85 | °C   |

**(3)Electrical Characteristics (Tj=25°C,VCC=18V,Rt=12kΩ,unless otherwise specified)**

## Oscillator Section (RT pin)

| Item                            | Symbol | Conditions          | MIN. | TYP. | MAX. | Unit |
|---------------------------------|--------|---------------------|------|------|------|------|
| Switching oscillation frequency | Fosc   | Rt=12kΩ, Tj=25°C    | 171  | 190  | 209  | kHz  |
| Variation by supply voltage     | Fdv    | VCC=11V to 30V      | -2   | -    | +2   | %    |
| Variation by temperature        | FdT    | Tj= -40°C to +125°C | -    | 0.05 | -    | %/°C |

## Pulse Width Modulation Section (FB pin)

| Item                     | Symbol  | Conditions        | MIN.      | TYP. | MAX. | Unit |   |
|--------------------------|---------|-------------------|-----------|------|------|------|---|
| Source current of FB pin | IFB     | FB=0V             | -650      | -500 | -390 | μA   |   |
| Input threshold voltage  | VthFB0  | Duty cycle=0%     | 0.9       | 1.0  | 1.1  | V    |   |
|                          | VthFBM  | Duty cycle=DMAX   | 2.7       | 3.0  | 3.25 | V    |   |
| Maximum duty cycle       | DMAX    | FB=3.25V          | FA5604    | 43   | 46   | 49   | % |
|                          |         |                   | FA5605/06 | 67   | 70   | 73   |   |
| OLP threshold voltage    | Volpon  | OLP mode OFF → ON | 3.2       | 3.5  | 3.8  | V    |   |
|                          | Volpoff | OLP mode ON → OFF | 3.0       | 3.3  | 3.6  | V    |   |
| Hysteresis voltage width | Volphys |                   | 0.1       | 0.2  | 0.3  | V    |   |

## Frequency Control Section at Light Load (FB pin)

| Item                              | Symbol    | Conditions                | MIN.      | TYP. | MAX. | Unit |   |
|-----------------------------------|-----------|---------------------------|-----------|------|------|------|---|
| Input threshold voltage           | VthFBS1   | Light Load mode<br>OFF→ON | FA5604/05 | 1.65 | 1.80 | 1.95 | V |
|                                   |           |                           | FA5606    | 1.43 | 1.55 | 1.67 |   |
|                                   | VthFBS2   | Light Load mode<br>ON→OFF | FA5604/05 | 1.8  | 1.95 | 2.1  |   |
|                                   |           |                           | FA5606    | 1.53 | 1.65 | 1.77 |   |
| Difference of switching frequency | Foscdiff1 | RT=24kΩ<br>FB=VthFBS      | FA5604    | -15  | -7.5 | 0    | % |
|                                   |           |                           | FA5605/06 | -10  | -5   | 0    |   |
| Minimum switching frequency       | FoscS2    | FB=VthFB0                 | 24        | 30   | 39   | %    |   |
| Minimum on pulse width            | tminS     | FB=VthFB0                 | 300       | 400  | 500  | ns   |   |

## Current Sense Section (IS pin)

| Item                     | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|--------|------------|------|------|------|------|
| Input threshold voltage  | VthIS  |            | -183 | -170 | -157 | mV   |
| Source current of IS pin | IIS    | IS=0V      | -52  | -40  | -28  | μA   |
| Propagation delay time   | tpdIS  |            | 100  | 150  | 250  | ns   |

## ON/OFF, Soft-start Section (CS pin)

| Item                     | Symbol  | Conditions        | MIN.      | TYP. | MAX. | Unit |   |
|--------------------------|---------|-------------------|-----------|------|------|------|---|
| Charge current of CS pin | ICS0    | CS=0V             | -13       | -10  | -7   | μA   |   |
| ON/OFF threshold voltage | Vcson1  | OFF→ON            | 0.65      | 0.75 | 0.90 | V    |   |
|                          | Vcsoff1 | ON→OFF            | 0.50      | 0.60 | 0.75 | V    |   |
| Hysteresis voltage width | Vcshys1 |                   | 0.1       | 0.15 | 0.2  | V    |   |
| Soft-start input voltage | VthCS0  | Duty cycle = 0%   | 0V→VthCSM | 0.65 | 0.75 | 0.9  | V |
|                          |         |                   | VthCSM→0V | 0.5  | 0.6  | 0.75 |   |
|                          | VthCSM  | Duty cycle = DMAX | 2.75      | 3.0  | 3.25 | V    |   |

**Latch Protection Section (CS pin)**

| Item                    | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------|--------|------------|------|------|------|------|
| Latch threshold voltage | VthLAT |            | 6.6  | 7.3  | 7.7  | V    |
| Latch delay time        | TpdLAT |            | 35   | 50   | 70   | μs   |
| Clamp voltage of CS pin | VCSP   | ICS=2mA    | 13   | 15   | 17   | V    |

**Frequency Control Section at Overload (VF pin)**

| Item  | Symbol    | Conditions                | MIN.      | TYP. | MAX. | Unit |     |
|---|-----------|---------------------------|-----------|------|------|------|-----|
| Threshold voltage of frequency reducing at overload | VVF       | FB=open                   | 3.9       | 4.2  | 4.5  | V    |     |
| Switching frequency at overload                     | FoscL1    | Rt=12kΩ<br>FB=open, VF=5V | FA5604    | 145  | 165  | Fosc | kHz |
|   |           |                           | FA5605/06 | 155  | 180  | Fosc |     |
|   | FoscL2    | Rt=12kΩ<br>FB=open, VF=2V | FA5604    | 90   | 115  | 160  | kHz |
|   |           |                           | FA5605/06 | 110  | 140  | 170  |     |
| Difference of switching frequency                   | FoscDiff2 | Rt=24kΩ<br>FB=open, VF=5V | FA5604    | -15  | -7.5 | 0    | %   |
|   |           |                           | FA5605/06 | -10  | -5   | 0    |     |
| VF voltage at timer enable                          | VFcstim   |                           | 2.7       | 3.0  | 3.3  | V    |     |
| VF voltage at timer reset                           | VFcstmr   | FB=open, VF increasing    | 3.15      | 3.5  | 3.85 | V    |     |
| Hysteresis width at timer                           | Vhyscst   | VFcstmr-VFcstim           | 0.45      | 0.5  | 0.55 | V    |     |
| Input bias current at VF pin                        | IVF       | VF=0V                     | -2        | -0.5 | -    | μA   |     |

**Hiccup Section (CS pin)**

| Item   | Symbol  | Conditions           | MIN.      | TYP. | MAX. | Unit |    |
|--|---------|----------------------|-----------|------|------|------|----|
| Threshold voltage of timer   | VcstimH |                      | 4.9       | 5.7  | 6.5  | V    |    |
|  | VcstimL |                      | 3.3       | 3.8  | 4.3  | V    |    |
| Voltage width of timer   | VcstimW |                      | 1.5       | 1.9  | 2.3  | V    |    |
| Difference voltage between timer-upper voltage and Latch threshold voltage | VcsdLT  | VCC=18V, Ccs=10nF    | 0.9       | 1.6  | 2.5  | V    |    |
| Timer Charge current   | Icschg2 |                      | -13       | -10  | -7   | μA   |    |
| Timer Charge current   | Icsdis2 |                      | 7         | 10   | 13   | μA   |    |
| Delay time of OLP  | Tolp1   | VCC=18V, Ccs=10nF    | 179       | 256  | 333  | ms   |    |
| The time of OLP  | Tolp2   | VCC=18V,<br>Ccs=10nF | FA5604/06 | 1225 | 1792 | 2330 | ms |
|  |         |                      | FA5605    | 2688 | 3840 | 4992 |    |
| Time ratio of OFF/ON time  | Konoff  | Tolp2/Tolp1          | FA5604/06 | -    | 7    | -    | -  |
|  |         |                      | FA5605    | -    | 15   | -    |    |

**Under Voltage Lock Out Section (VCC pin)**

| Item                       | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|--------|------------|------|------|------|------|
| Startup threshold voltage  | VCCON  |            | 15.5 | 17.5 | 19.5 | V    |
| Shutdown threshold voltage | VCCOFF |            | 8.5  | 9.7  | 10.5 | V    |
| UVLO hysteresis width      | VCCHYS |            | 6    | 7.8  | 10   | V    |



**Output Driver Section (OUT pin)**

| Item                      | Symbol | Conditions          | MIN. | TYP. | MAX. | Unit |
|---------------------------|--------|---------------------|------|------|------|------|
| Low level output voltage  | VOL    | IOL=100mA, VCC=18V  | -    | 0.7  | 1.5  | V    |
| High level output voltage | VOH    | IOH=-100mA, VCC=18V | 15   | 16.5 | -    | V    |
| Rise time                 | Tr     | CL=1nF (OUT pin)    | 20   | 40   | 100  | ns   |
| Fall time                 | Tf     | CL=1nF (OUT pin)    | 15   | 30   | 70   | ns   |

**Over Voltage Protection Section (VCC pin)**

| Item                              | Symbol | Conditions      | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------|-----------------|------|------|------|------|
| VCC pin clamp voltage at OFF mode | VzdL   | Icc=250 $\mu$ A | 14.5 | 15.5 | 16.5 | V    |

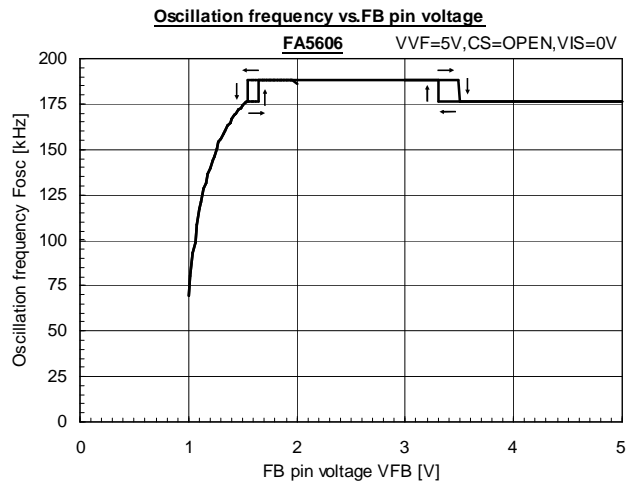
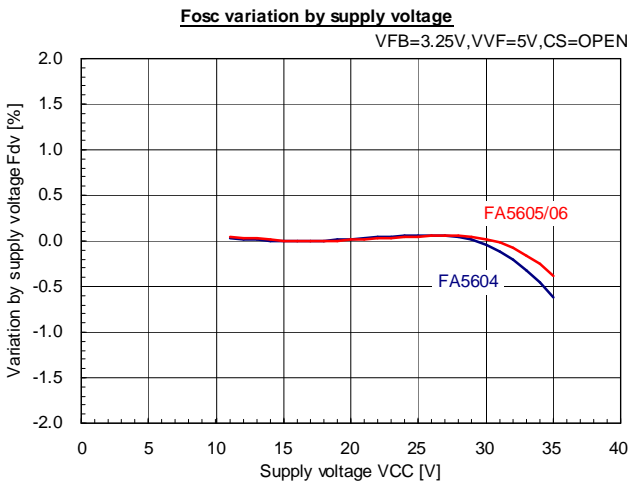
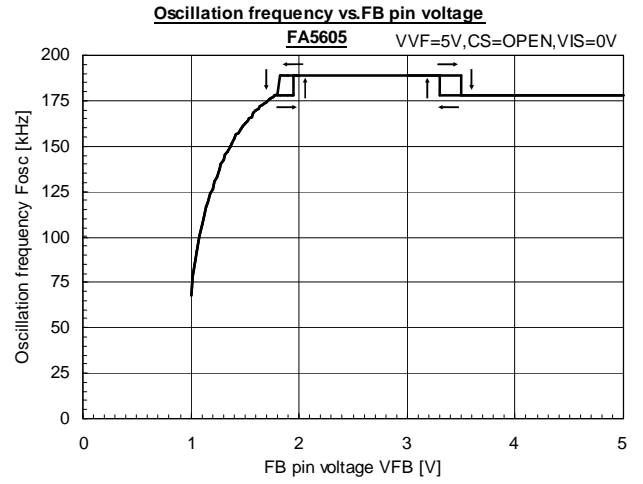
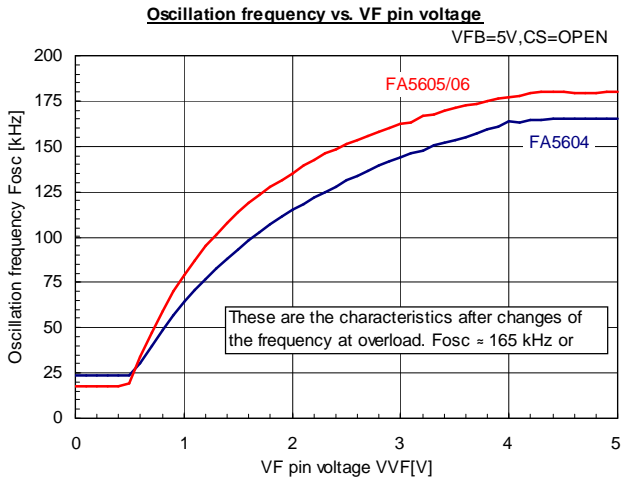
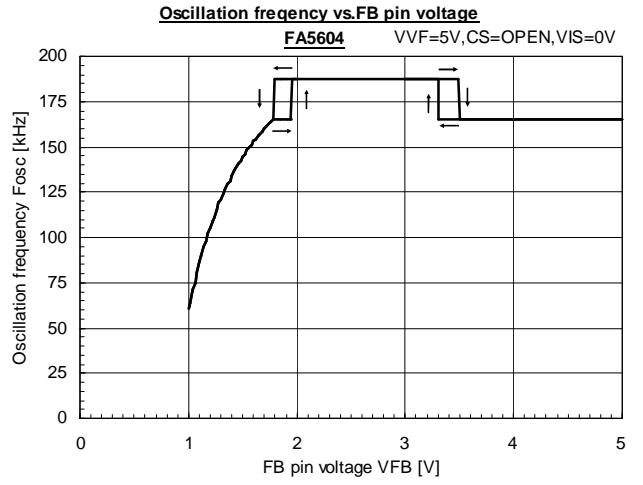
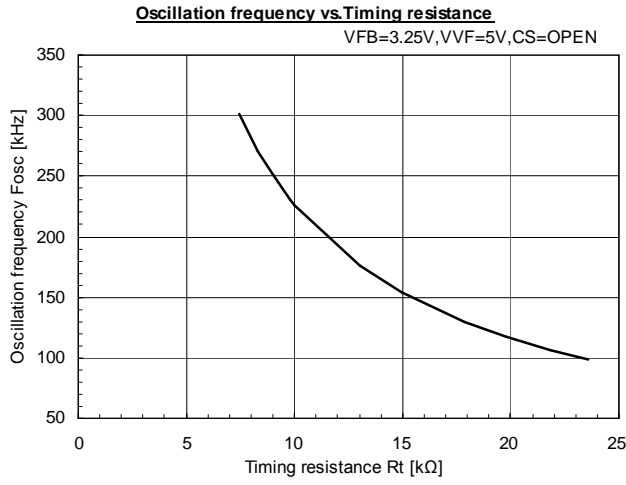
**Power Supply Current Section (VCC pin)**

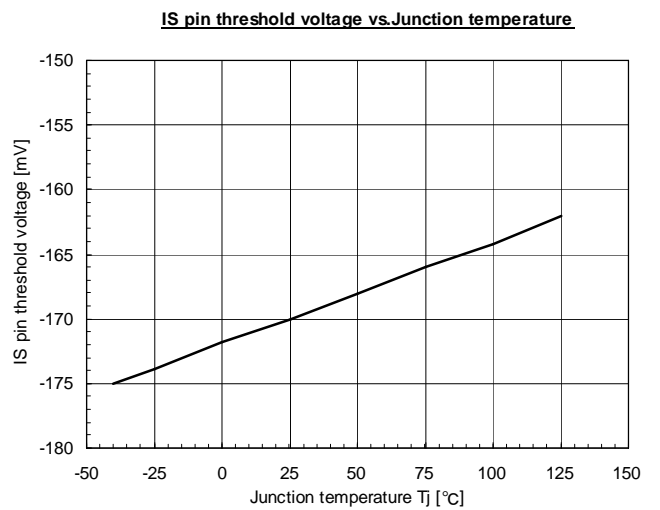
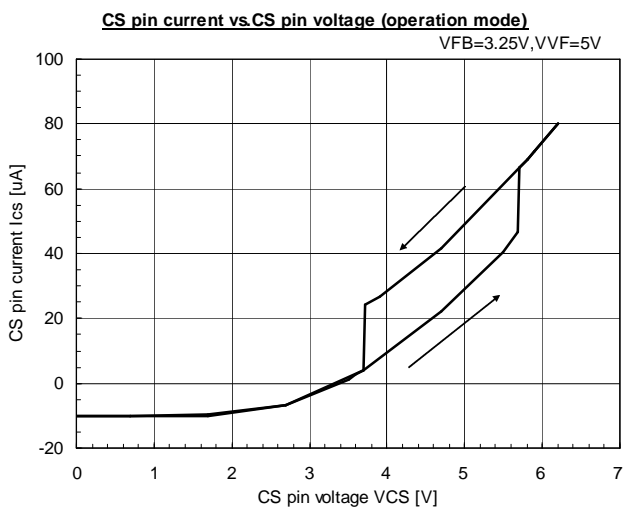
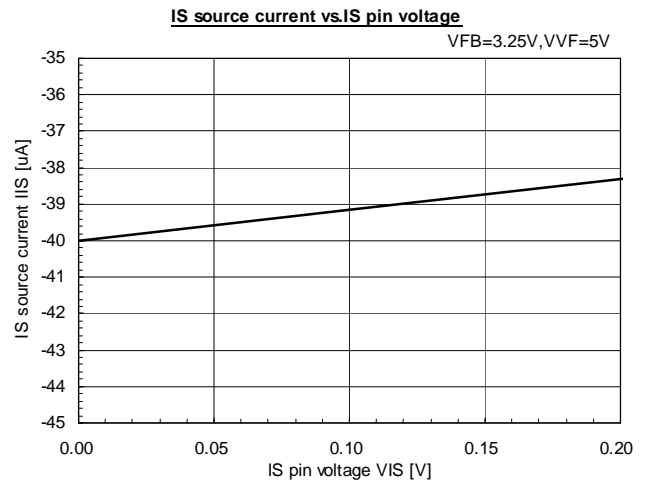
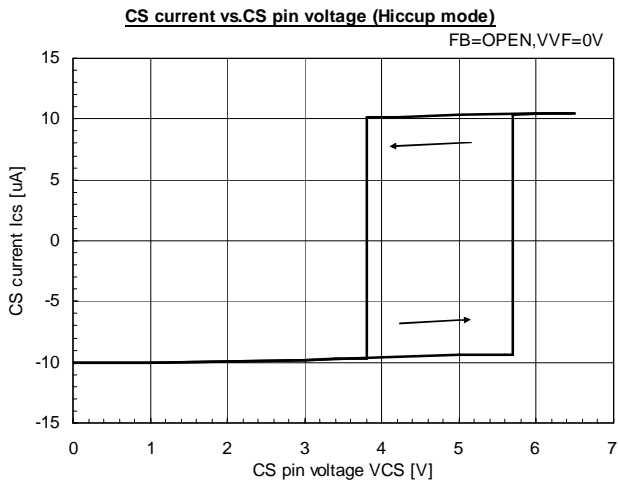
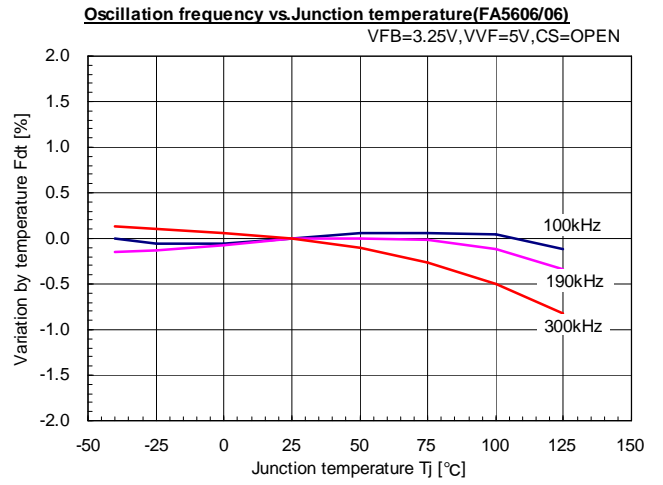
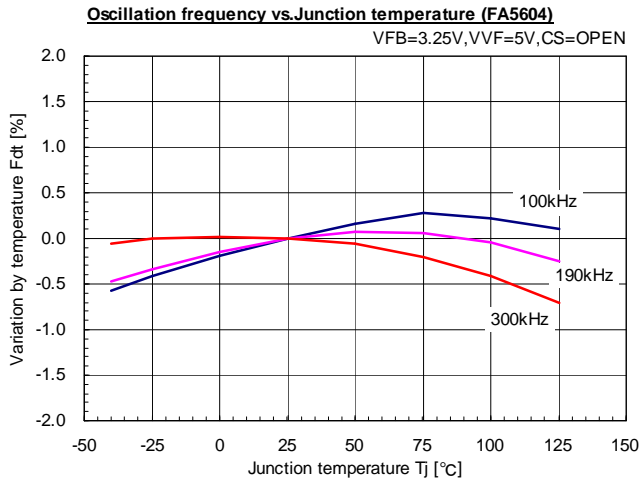
| Item                                 | Symbol  | Conditions                                    | MIN. | TYP. | MAX. | Unit    |
|--------------------------------------|---------|---|------|------|------|---------|
| Stand-by current                     | IccSTB  | VCC=14V                                       | -    | -    | 2    | $\mu$ A |
| Start-up current                     | IccST   | VCC = Start threshold voltage                 | -    | 14   | 35   | $\mu$ A |
| Steady operating mode supply current | IccOP1  | At No Load, VCC=18V, FB=3.25V, VF=5V, CS=open | -    | 1.6  | 3.0  | mA      |
| OFF mode supply current              | Iccoff  | At No Load, VCC=14V, FB=0V, VF=0V, CS=0V      | -    | 195  | 250  | $\mu$ A |
| CS timer-off mode supply current     | Iccoff1 | VCC=14V                                       | -    | 190  | 240  | $\mu$ A |
| Latch-mode supply current            | IccLAT1 | VCC=11V                                       | -    | 185  | 240  | $\mu$ A |
|                                      |         | VCC=14V                                       | -    | 190  | 240  | $\mu$ A |

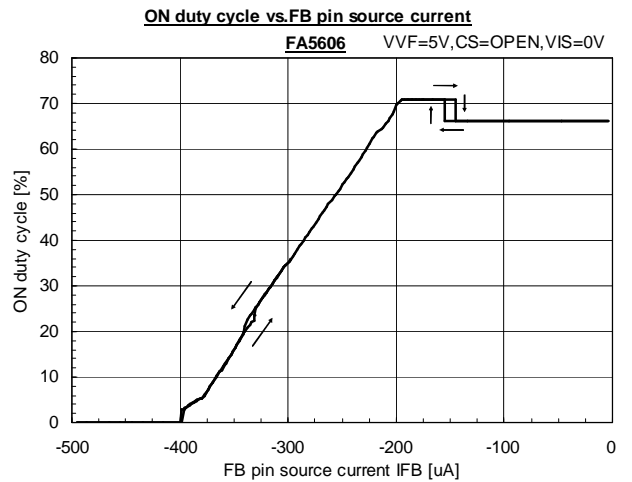
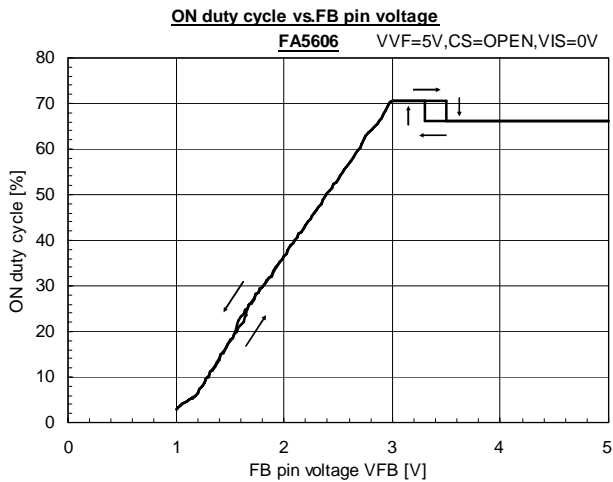
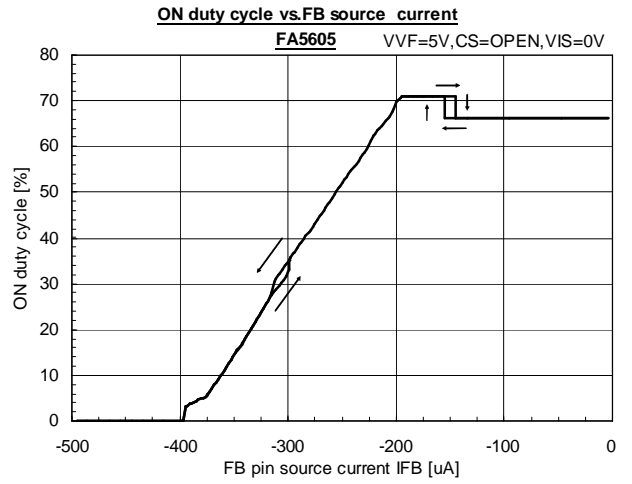
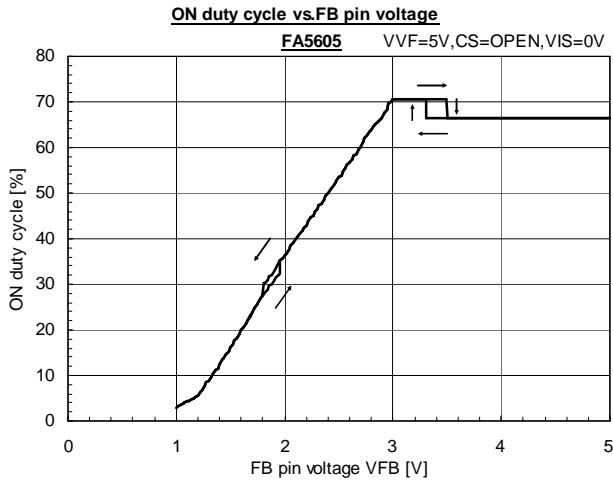
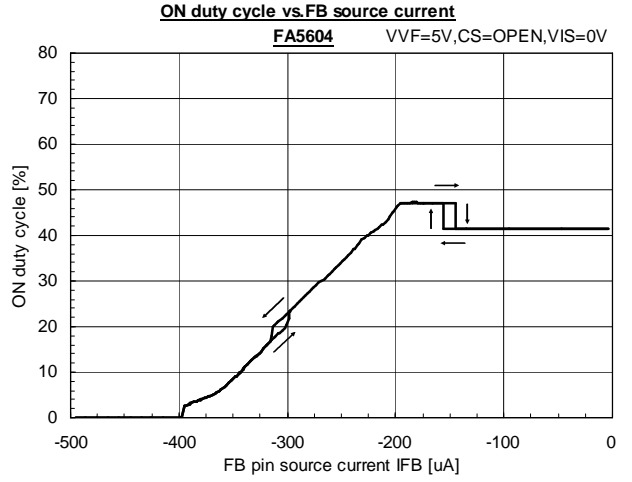
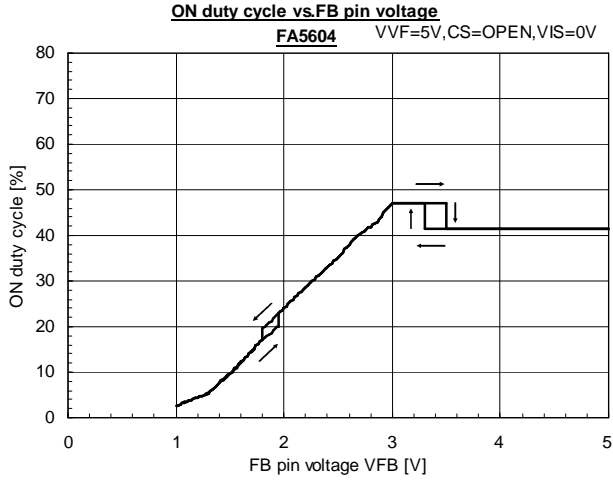
**8. Characteristic curve**

Ta=25°C, VCC=18V, Rt=12kΩ, unless otherwise specified

Parts tolerance and characteristics are not defined in all application described in this Data book.

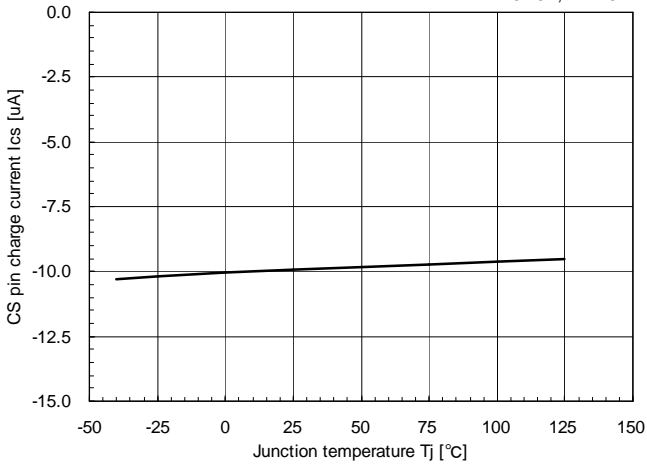






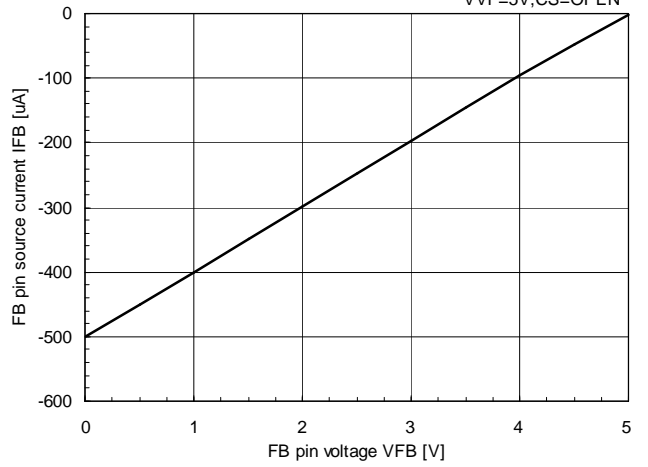
**CS pin charge current vs. Junction temperature**

VFB=3.25V, VVF=5V



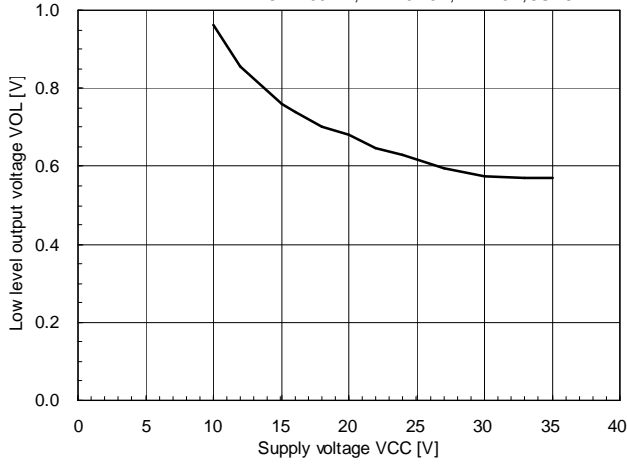
**FB pin source current vs. FB pin voltage**

VVF=5V, CS=OPEN



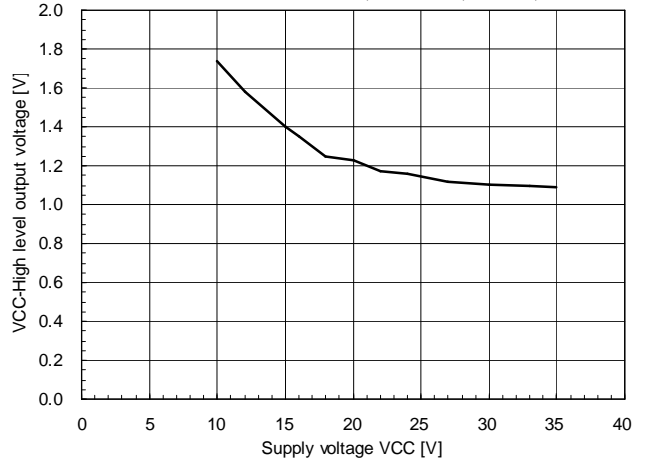
**Low level output voltage vs. Supply voltage**

IOL=100mA, VFB=3.25V, VVF=5V, CS=OPEN

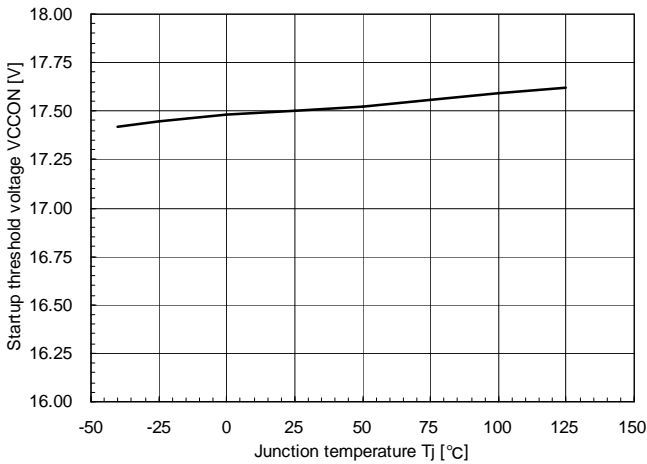


**High level output voltage vs. Supply voltage**

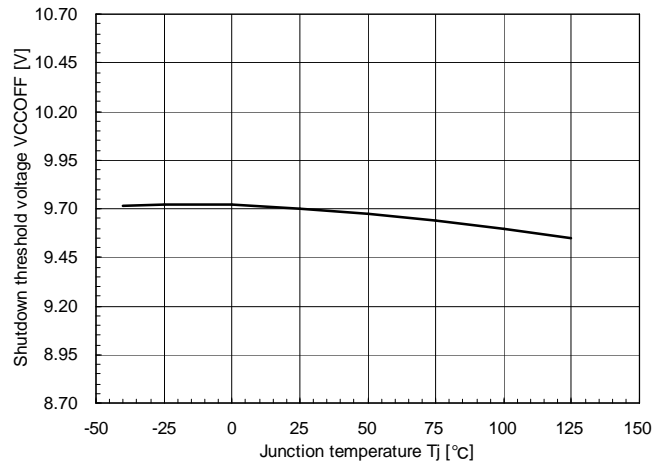
IOH=-100mA, VFB=3.25V, VVF=5V, CS=OPEN

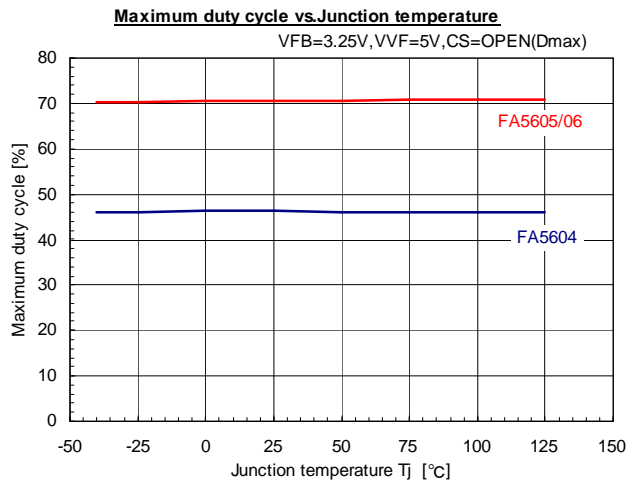
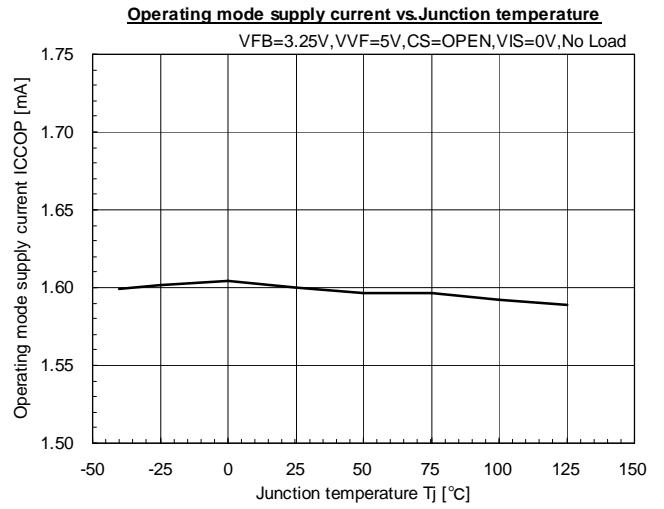
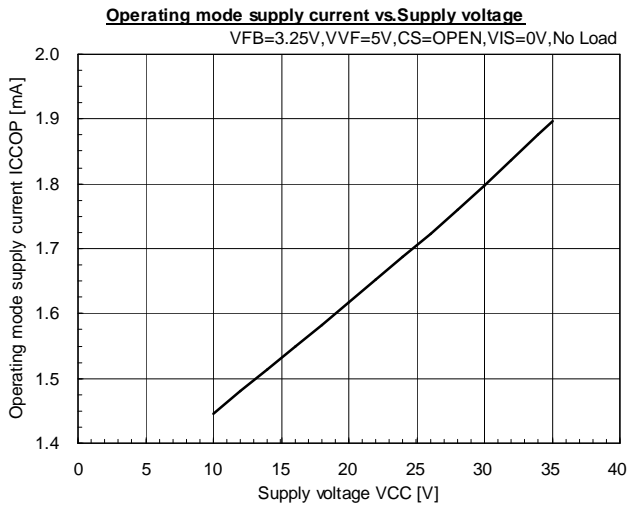


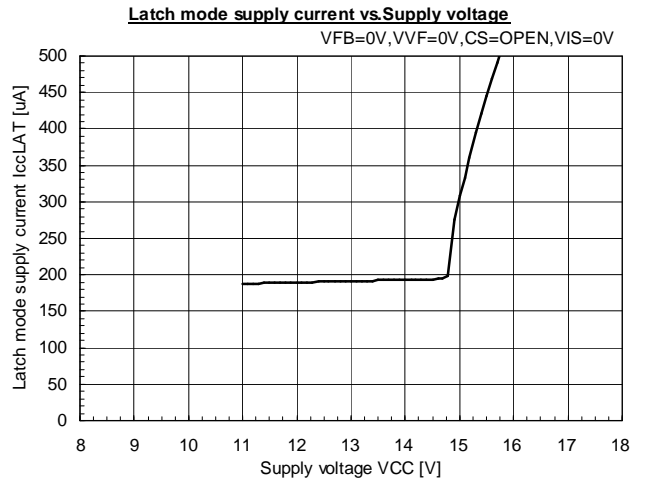
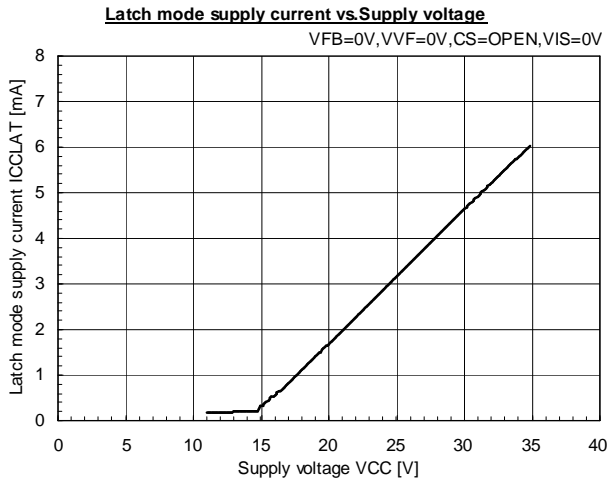
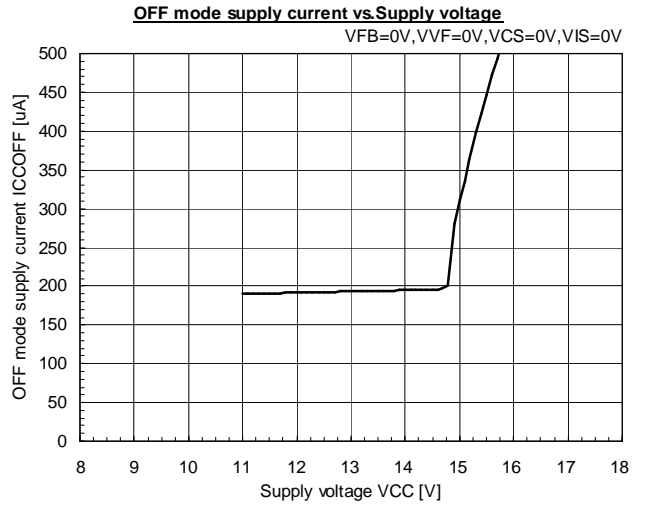
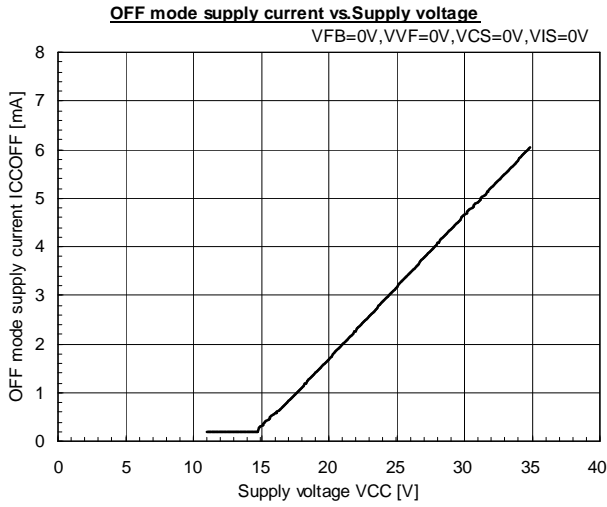
**Startup threshold voltage vs. Junction temperature**



**Shutdown threshold voltage vs. Junction temperature**







9. Description of each circuit

(1)Oscillator

A desired oscillation frequency can be set by the value of the resistor connected to the RT pin (Fig.1 recommended value is 100 kHz to 300 kHz). The built-in capacitor voltage oscillates between about 3V and 1V, with almost the same charging and discharging gradients (Fig.2).

The oscillator waveform cannot be observed from the outside because the oscillator output is not pinned out. The oscillator output is connected to a PWM comparator.

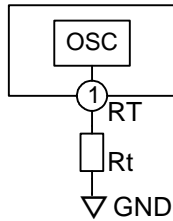


Fig.1

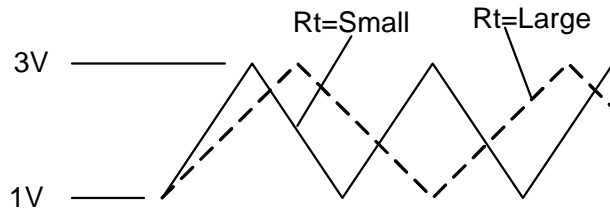


Fig.2

This IC has the function that reducing the power consumption by decreasing frequency at light load. It according to the value of the FB pin voltage at light load (Fig.3). When the FB pin voltage is 1V (typ.), the switching frequency decreases to about 30% down of the set frequency. When at the overload, it corrects current limiting by decreasing frequency. The minimum switching frequency is about 10% down of the set frequency.

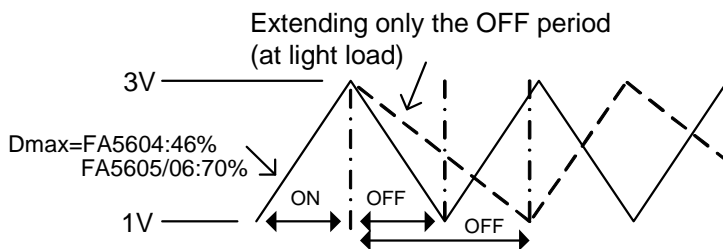


Fig.3

As shown in Fig.4 (Fosc-VFB characteristics graph), there is a little difference at the point before the frequency is reduced. Check that this is not a problem for actual use.

Because this IC adopts the frequency reduction method in which only the off period is extended, if the frequency is reduced at overload, the ON duty is also reduced, and therefore the output voltage is reduced. Consequently, the load current is reduced at the point in which it enters the drooping characteristics at overload (Fig 5).

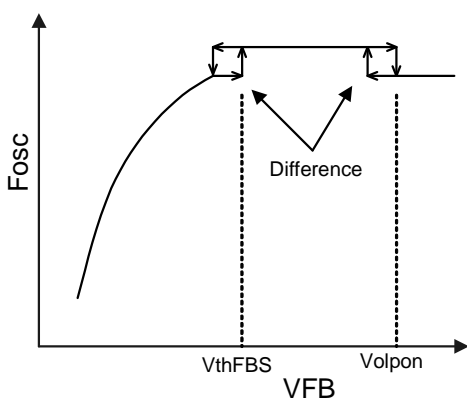


Fig.4

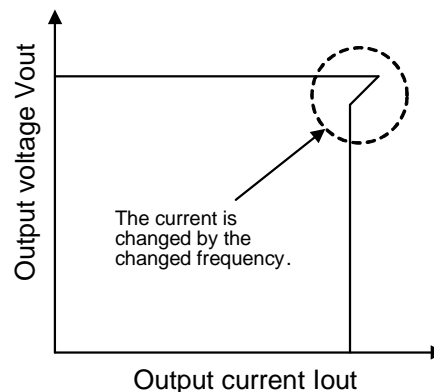


Fig.5



**(2)PWM comparator**

Fig.6 shows the PWM comparator timing chart. The PWM comparator has three inputs. Oscillator output ① is compared with CS pin voltage ② and FB pin voltage ③. The lower of two inputs ② and ③ has priority and compared with oscillator output ①. While the voltage is lower than the oscillator output, the PWM comparator output is high. While the voltage is higher than the oscillator output, the PWM comparator output is low.

The OUT pin of the IC is controlled so that it is H at the bottom of triangular wave oscillation waveforms (Output MOSFET is ON) and L when the PWM comparator output is set to H (Output MOSFET is OFF).

When the IC is started up, CS pin voltage ② controls soft start operation. The output pulse then begins to widen gradually. During normal operation, the output pulse width is determined within the maximum duty cycle (FA5604:46%, FA5605/06:70%) set by FB pin voltage ③, to stabilize the output voltage.

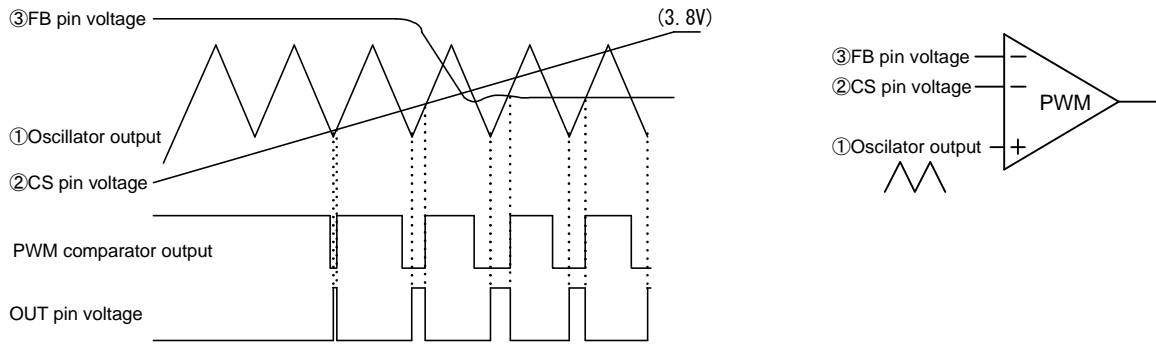


Fig.6

**(3)CS pin circuit**

The CS pin connects to the capacitor Ccs. The CS pin voltage varies depending on the charging voltage of this capacitor Ccs (Fig.7).

When the power is turned on, the constant current source (10μA) begins to charge capacitor Ccs. Because of that, the CS terminal voltage gradually increases as shown in Fig.6. The CS pin voltage is connected to the PWM comparator, which is characterized to make output based on the lowest of input voltages. The device enters soft-start mode while the CS pin voltage is between 1.0V and 3.0V. During normal operation, the CS pin voltage is clamped at 3.8V by internal zener diode. If the output voltage drops due to an overload and the VF pin voltage become 3V or less, the clamp voltage 3.8V is canceled and the CS pin voltage rises. The CS pin voltage is oscillate between 3.8V and 5.7V, and determined the time ratio of OLP hiccup.

Moreover, the CS pin is connected to latch comparator. If the CS pin voltage rises to 7.3V (50μsec) or more, comparator toggles to turn off, thereby shutting the output down. Since the CS pin is also connected to ON/OFF comparator, this circuit can be turned off to shut the output down by dropping the CS pin voltage below 0.60V.

In this way, the CS pin can be used for soft-start, overload output shutdown, external latch, ON/OFF control by varying the voltage (Fig.8).

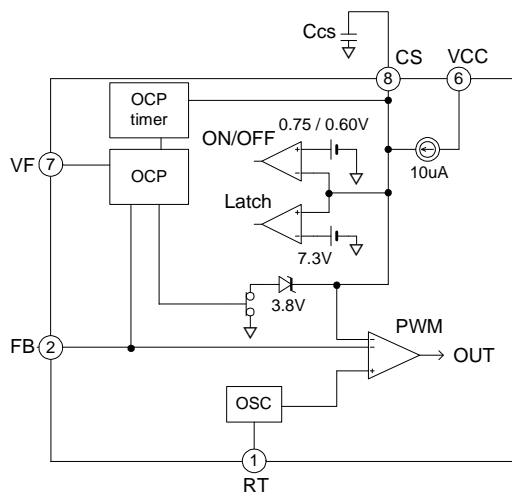


Fig.7

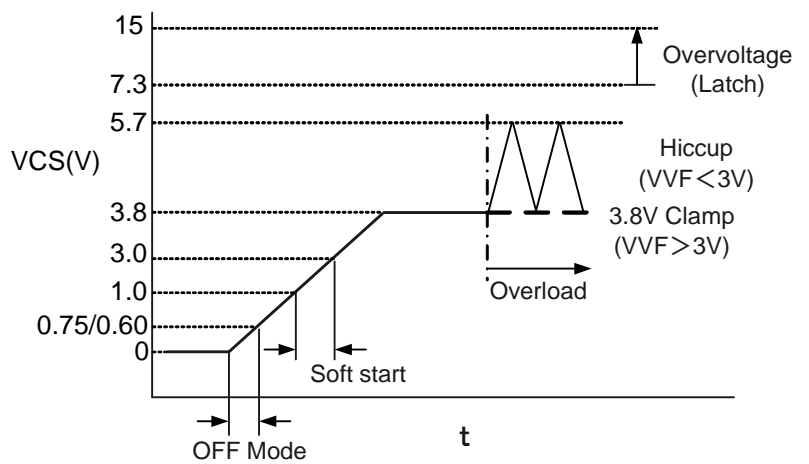


Fig.8

Further details on the above four major functions of the CS pin are given below.

**(i) Soft start function**

Fig.9 shows the soft start operation timing chart. The CS pin is connected to capacitor Ccs. When the power is turned on, the constant current source (10μA) begins to charge the capacitor. As shown in the timing chart, the CS pin voltage rises slowly. The CS pin is connected to the IC internal PWM comparator, and then the comparator output pulse slowly widens to cause a soft start as shown in the timing chart. After the soft start, the CS pin voltage is clamped at 3.8V by internal zener diode.

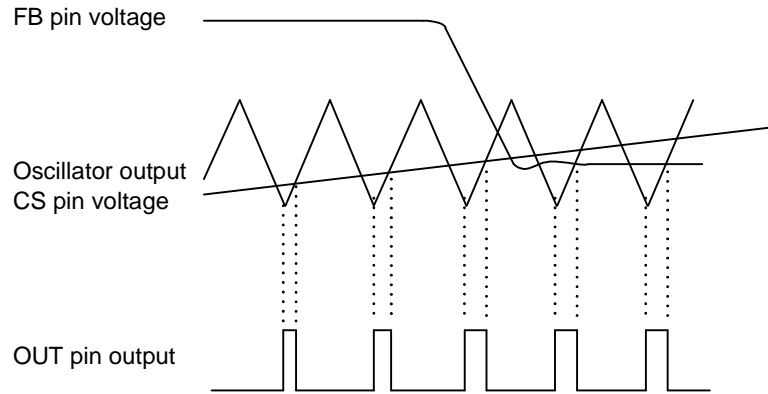
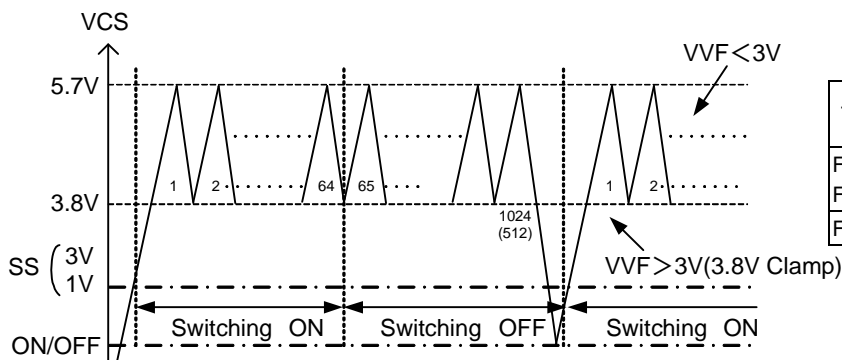


Fig.9

**(ii) Overload shutdown function**

Fig. 10 shows the timing chart of the CS terminal voltage (VCS) under overload condition. To achieve intermittent operation at overvoltage, apply a voltage proportional to the output voltage to VF terminal. If the output voltage is reduced by overvoltage or the like, the VF terminal voltage is reduced. If the VF terminal voltage is 3 V or more, the CS terminal voltage is clamped at 3.8 V and perform an output drooping operation. Subsequently, when the output voltage is reduced due to overload, short circuit, or the like, and the VF terminal voltage becomes less than 3 V, the CS terminal voltage oscillates between 3.8 V and 5.7 V. Intermittent operations are performed at switch-on during the count period of 1 to 64 and at switch-off during the count period of 65 to 512 (switching period ratio: 64/448 = 1 : 7) at FA5604/06, and at switch-on during the count period of 1 to 64 and at switch-off during the count period of 65 to 1024 (switching period ratio: 64/960 = 1 : 15) at FA5605. The intermittent function is achieved by three terminals: CS, FB, and VF terminals. For the detailed description, see item (6) below.



| Type             | Switching ON | Switching OFF | ON:OFF |
|------------------|--------------|---------------|--------|
| FA5604<br>FA5606 | 0~64         | 65~512        | 1 : 7  |
| FA5605           | 0~64         | 65~1024       | 1 : 15 |

Fig.10

**(iii) External latch function**

When the CS pin voltage exceeds 7.3V (50μsec), the IC is stopped the switching. If the VCC voltage reduced to 9.7V (typ.) (ON threshold voltage of UVLO) or less, the latch hold mode can be released.

After the latch hold mode, the CS pin voltage becomes 7.3V or less is maintained to this mode. However, it is necessary to keep supplying the consumption current 190μA (VCC=14V) from input Vin through the startup resistor.

When the current supplied from Vin is less than the consumption current of IC, VCC reduced to the UVLO voltage and the latch hold mode cannot be maintained.

During normal operation, the CS pin voltage is clamped at 3.8V by internal zener diode. The VF pin is input to the voltage proportional to the output voltage

In normal operation, the CS pin voltage is clamped at 3.8V by internal zener diode with maximum sink current 100μA (max.). Therefore, to raise the CS pin voltage to 7.3V or more, 200μA or a higher current needs to be supplied from the optocoupler. Set the current input to the CS pin to 2 mA or less.

**(iv) ON/OFF function**

The IC can be turned ON/OFF control via an external signal applied to the CS pin. Fig.11 shows the ON/OFF control circuit, and Fig.12 is a timing chart.

The IC is turned off when the CS pin voltage is externally made to drop below 0.60V. The output enters Low voltage state. Required IC current consumption during shutdown is 185μA (Vcc=10.5V), and this current must be supplied through the start up resistor. If the supplied current from Vin is lower than the current consumption, Vcc is reduced to the UVLO voltage and the turned off state for CS pin cannot be maintained.

In case of turning on operation, open the CS pin and the CS pin voltage exceeds 1.0V. So the power supply begins operation with soft-start.

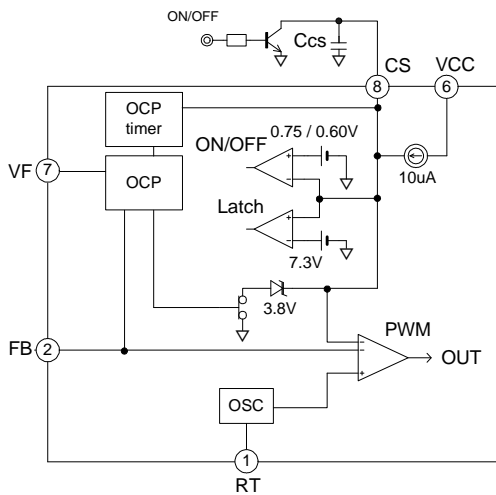


Fig.11

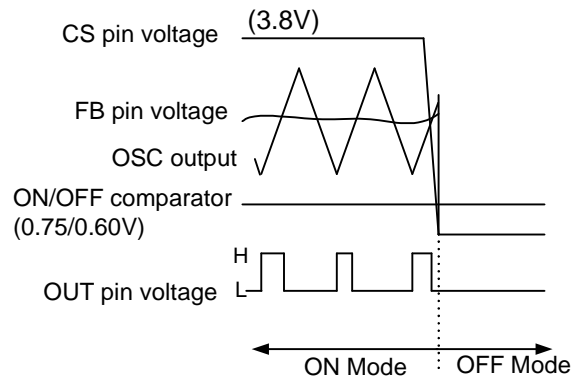


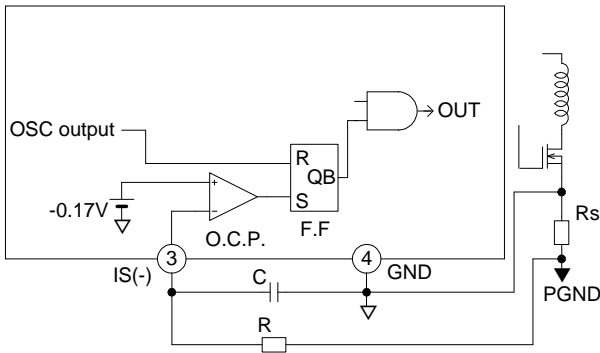
Fig.12

**(4)Overcurrent limiting circuit**

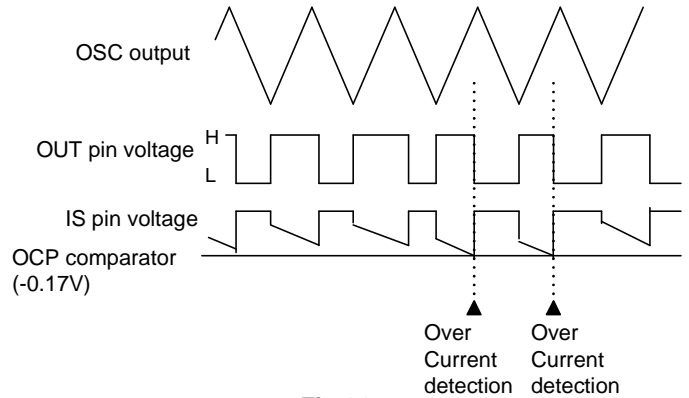
This circuit detects the peak value of every drain current pulse (pulse by pulse method) of the main switching MOSFET to limit the overcurrent, and the detection threshold voltage is -0.17V with respect to the ground level. **Fig. 13** shows overcurrent limiting circuit, and **Fig.14** is the overcurrent timing chart.

The drain current of the MOSFET is converted to voltage by resistor  $R_s$  and fed to the IS pin of the IC. If the detection voltage becomes -0.17V or less, the O.C.P comparator output is high, and the RS-FF output QB to Low. The OUT of this IC becomes L level at the moment, the MOSFET is turned off to shut off the current. The flip-flop output is reset on the next cycle to turn on the output again. This operation is repeated to limit the overcurrent.

If the overcurrent limiting circuit malfunctions due to noise, place an RC filter between the IS pin and MOSFET as shown in **Fig. 13**. (See item 6 in "Design advice")



**Fig.13**

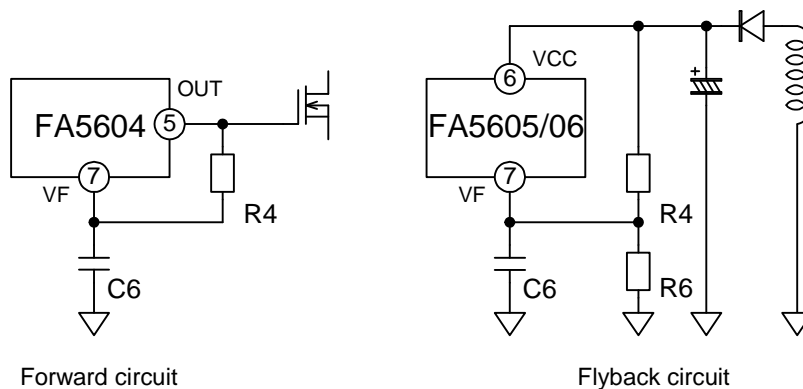


**Fig.14**

**(5)Overload protection circuit (switching frequency control by VF pin)**

The voltage proportional to the output voltage is input the VF pin. If the output voltage drops due to an overload and so on, the FB pin voltage rises and the VF pin voltage decreases. When the FB pin voltage exceeds 3.5V, IC is operating the OLP mode. The VF pin voltage becomes 4.2V or less, the oscillatory frequency decreases according to the voltage value. In adds to overcurrent limiting (preceding clause 4), overload protect by decreasing the oscillatory frequency (See item 5 in "Design advice")

To a voltage proportional to the output voltage, apply the OUT terminal voltage smoothed in the case of the forward circuit, or apply the VCC voltage in the case of the flyback circuit (see **Fig. 15**).



**Fig.15**

**(6)Overload protection circuit**

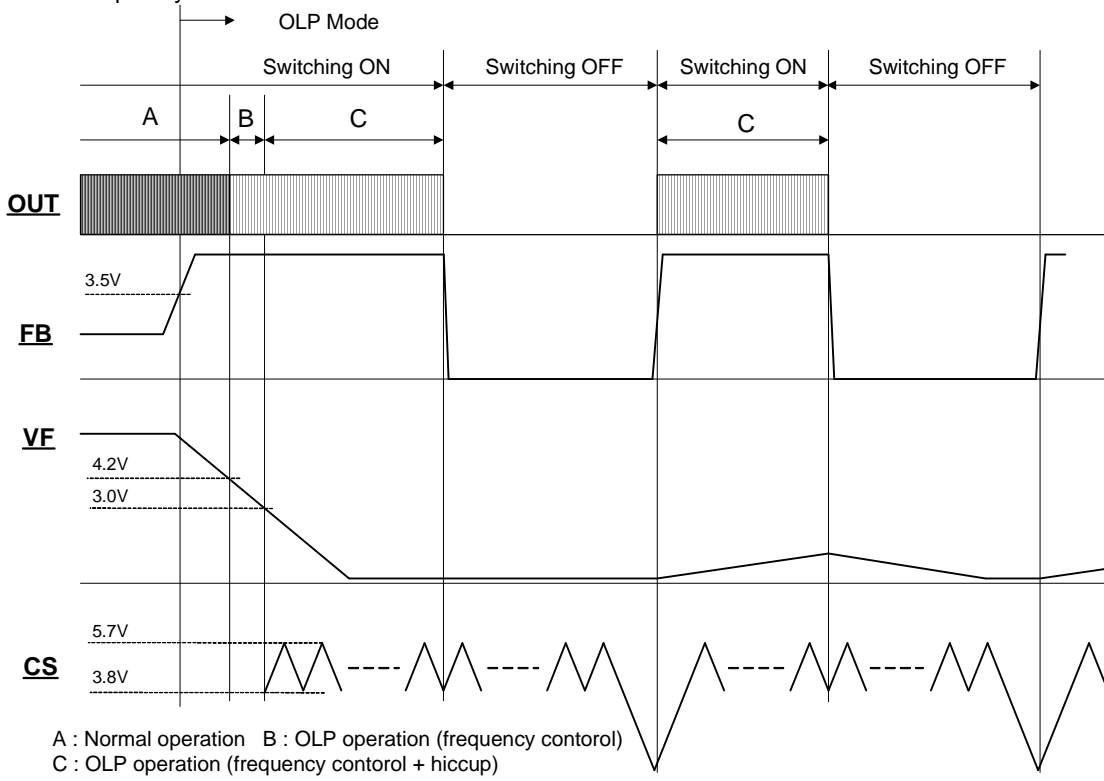
The IC contains an overload protection circuit (operation that switching turned ON/OFF in fixed time ratio). **Fig.16** shows a timing chart at overload.

During normal operation, the CS pin voltage is clamped at 3.8V by internal zener diode. The VF pin is input to the voltage proportional to the output voltage.

If the output voltage drops due to an overload and so on, the FB pin voltage rises to raise the output voltage. If the FB pin voltage exceeds 3.5V, the IC toggles to overload protection (OLP) mode. The VF pin voltage decreases at the same time as output voltage. If the VF pin voltage reduced to 4.2V or less, switching frequency control is began at overload. Moreover, if the VF pin voltage becomes 3.0V or less, the clamp voltage is canceled and the capacitor Ccs, which is connected the CS pin, is charged by constant current source (10μA).

If the CS pin voltage rises to 5.8V or more, it toggles to discharge mode, and the capacitor is discharged by constant current source (10μA). If the CS pin voltage reduced to 3.9V or less again, it toggles to charge mode, and the capacitor is charged.

The CS terminal performs an oscillation operation between 3.8 V and 5.7 V by repeating the above operation. The intermittent operations are performed by counting the oscillation waveforms inside the IC and by making a setting so that the count period of 1 to 64 is the switching operation period and the count period of 65 to 512 (FA5604/06) or 65 to 1024 (FA5605) is the switching shutdown period (switching-on period: switching-off period: 64:448 = 1:7 or 64:960 = 1:15). The operation frequency during the intermittent operation is under the condition in which the frequency is reduced.



**Fig.16**

**(7)Undervoltage lockout circuit (U.V.L.O)**

The IC incorporates a circuit that prevents the IC from malfunctioning when the supply voltage drops. When the supply voltage is raised from 0V, the IC starts operation with VCC=17.5V (typ.). If the supply voltage drops, the output is shut down when VCC =9.7V (typ.). When the undervoltage lockout circuit operates, the output of the the OUT and CS pins go low to reset the IC.

**(8)Output circuit**

The IC contains a push-pull output stage and can directly drive the MOSFET. The absolute maximum rating of OUT pin peak current is +1.0A/-0.5A. But when using in actual circuit, the output peak current depends on the characteristics of the MOSFET, the resistance between the OUT pin and the MOSFET, supply voltage, temperature conditions.

The output current causes loss of the output stage. The total loss caused by the operating current and the output current should be within the ratings in actual circuit. (See item 11 in "Design advice")

If the circuit turned off by undervoltage lockout circuit, the output of OUT pin become low level and the MOSFET is shut down.

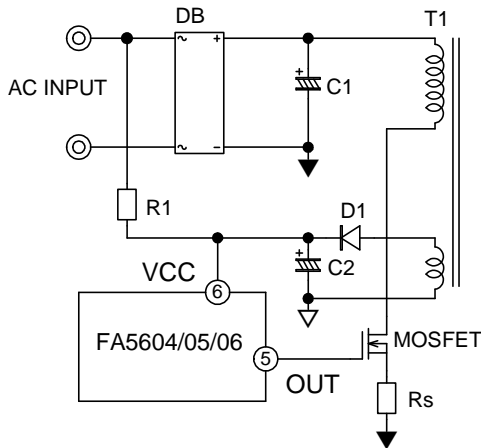
**10. Design advice**

**(1)Deciding the startup circuit**

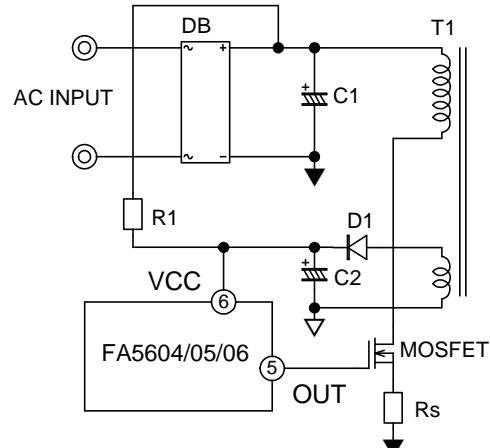
The connection methods of the startup circuit are as follows: connecting the starting resistor R1 before rectification (AC line) (**Fig. 17**); connecting the starting resistor R1 after rectification (DC line) (**Fig. 18**).

When connecting the starting resistor before rectification, if the latch operates, a current applied to the IC from the starting resistor is stopped by stopping the AC input, and the latch can be reset in a significantly short time.

On the other hand, if connecting the starting resistor after rectification, because a current is applied to the IC from the smoothing capacitor C1 of the main circuit through the starting resistor even if the AC input is stopped, it takes time to reset the latch.



**Fig.17**

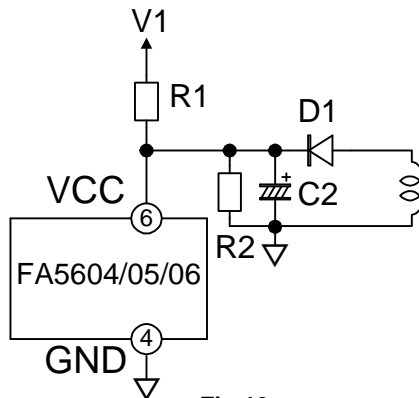


**Fig.18**

If it is necessary to set the startup and shutdown voltages, connect the resistor R2 between the VCC and the GND as shown in **Fig. 19**.

When connecting only the starting resistor R1, if setting a relatively large value for the starting resistor R1, the latch release voltage is more than the starting voltage. Under this condition, if the input voltage is reduced for some reason when the latch is stopped, release of the latch and startup may be performed repeatedly.

It is recommended to insert the resistor R2 between the VCC and the GND in order to avoid this phenomenon.



**Fig.19**

The following are the points for setting the starting resistance.

Because the consumption current of the IC is low due to adoption of the CMOS process, it is possible to set a large value for the starting resistance. When determining the value of the starting resistance, the following three conditions shall be satisfied:

- (a) Start the IC when turning on the power.
- (b) Supply the IC consumption current at latch operation to maintain the latch condition.
- (c) Supply the IC consumption current during off-state of the on-off function to maintain the off-state.

Note that these are the minimum conditions for using this IC and it is necessary to determine the value considering the starting time required for the setting.

**(1-1) If the startup/shutdown voltages are not set**

If the startup/shutdown voltages are not set, connect only the starting resistor R1. At this time, the starting resistor R1 shall satisfy the following three relational expressions. Set a relatively small value for R1 considering the temperature characteristics and the like.

(a) To supply 35  $\mu$ A (max) of the startup current at 19.5 V (max) of the on threshold voltage of UVLO:

$$\text{(Condition for startup)} \quad R1 < \frac{V1 - 19.5}{0.035} \quad \dots\dots (1)$$

(b) To supply 230  $\mu$ A (max) of the IC consumption current ( $V_{CC} = 10.5$  V) during the latch operation:

$$\text{(Condition for the latch)} \quad R1 < \frac{V1 - 10.5}{0.23} \quad \dots\dots (2)$$

(c) To supply 250  $\mu$ A (max) of the IC consumption current ( $V_{CC} = 10.5$  V) during off-state of the on-off function:

$$\text{(Condition for on-off state)} \quad R1 < \frac{V1 - 10.5}{0.25} \quad \dots\dots (3)$$

Where,

R1: starting resistance [k $\Omega$ ]

If connecting the starting resistor before rectification (AC line),  $V_{IN}$  is:  $V1 = \frac{\sqrt{2}}{\pi} \times V_{ac}$

If connecting the starting resistor after rectification (DC line),  $V_{IN}$  is:  $V1 = \sqrt{2} \times V_{ac}$

( $V_{ac}$  = an effective value of the AC input voltage)

Example: On the condition of startup at  $V_{ac} = 80$  V ( $V_{IN} = 113$  V) or less when connecting the starting resistor after rectification

$$\text{Condition for startup: } R1 < \frac{113 - 19.5}{0.035} \quad R1 < 2.7M\Omega$$

$$\text{Condition for maintaining the latch: } R1 < \frac{113 - 10.5}{0.23} \quad R1 < 446k\Omega$$

$$\text{Condition for maintaining the off-state: } R1 < \frac{113 - 10.5}{0.25} \quad R1 < 410k\Omega$$

Therefore, 400k $\Omega$  or less of the starting resistance is required.

In the case of  $R1 = 200$  k $\Omega$ :

The approximate starting voltage is:  $V_{IN} = 0.035 \times 200 + 19.5 = 26.5V$

The approximate latch release voltage is:  $V_{IN} = 0.23 \times 200 + 10.5 = 56.5V$

As shown above, the latch release voltage is more than the starting voltage. If the input voltage is reduced for some reason when the latch is stopped, startup and release of the latch are performed repeatedly.

If the latch release voltage is less than the starting voltage under the above condition, the starting resistance is about 40 k $\Omega$  or less and a large loss results.

If neither the latch operation nor the on-off function is not used, it is enough to satisfy only the formula (1)

**(1-2) If the startup/shutdown voltages are set**

If the startup/shutdown voltages are set, connect the resistor R2 between the starting resistor R1 and the VCC-GND as shown in **Fig. 19**. At this time, the starting resistor R1 shall satisfy the following three relational expressions. Set a relatively small value for R1 considering the temperature characteristics and the like.

(a) To supply 35  $\mu$ A (max) of the startup current at 19.5 V (max) of the on threshold voltage of UVLO:

$$\text{(Condition for startup)} \quad R1 < \frac{V1 - 19.5}{0.035 + \frac{19.5}{R2}} \quad \dots (4)$$

(b) To supply 230  $\mu$ A (max) of the IC consumption current (VCC = 10.5 V) during the latch operation:

$$\text{(Condition for the latch)} \quad R1 < \frac{V1 - 10.5}{0.23 + \frac{10.5}{R2}} \quad \dots (5)$$

(c) To supply 250  $\mu$ A (max) of the IC consumption current (VCC = 10.5 V) during off-state of the on-off function:

$$\text{(Condition for on-off state)} \quad R1 < \frac{V1 - 10.5}{0.25 + \frac{10.5}{R2}} \quad \dots (6)$$

Where,

R1: starting resistance [k $\Omega$ ]

If connecting the starting resistor before rectification (AC line), VIN is:  $V1 = \frac{\sqrt{2}}{\pi} \times Vac$

If connecting the starting resistor after rectification (DC line), VIN is:  $V1 = \sqrt{2} \times Vac$   
(Vac = an effective value of the AC input voltage)

Example: On the condition that R2 = 22 k $\Omega$  and the startup at Vac = 80 V (VIN = 113 V) or less when connecting the starting resistor after rectification

$$\text{Condition for startup: } R1 < \frac{113 - 19.5}{0.035 + \frac{19.5}{22}} \quad R1 < 101k\Omega$$

$$\text{Condition for maintaining the latch: } R1 < \frac{113 - 10.5}{0.23 + \frac{10.5}{22}} \quad R1 < 145k\Omega$$

$$\text{Condition for maintaining the off-state: } R1 < \frac{113 - 10.5}{0.25 + \frac{10.5}{22}} \quad R1 < 141k\Omega$$

Therefore, 101k $\Omega$  or less of the starting resistance is required.

In the case of R1 = 100 k $\Omega$ :

$$\text{The approximate starting voltage is: } VIN = R1 \times \left( 0.035 + \frac{19.5}{R2} \right) + 19.5 = 100 \times \left( 0.035 + \frac{19.5}{22} \right) + 19.5 = 112V$$

$$\text{The approximate latch release voltage is: } VIN = R1 \times \left( 0.23 + \frac{10.5}{R2} \right) + 10.5 = 100 \times \left( 0.23 + \frac{10.5}{22} \right) + 10.5 = 81.2V$$

As shown above, the condition that the latch release voltage is less than the starting voltage is satisfied.

If neither the latch operation nor the on-off function is not used, it is enough to satisfy only the formula (4).



**(2)Determining the VCC capacitor value**

To properly start the power supply, a certain value is required for the value is required for the capacitor connected to the VCC pin.

Fig.20 shows the VCC voltage at startup when a proper value is given to the capacitor. When the input power is turned on, the capacitor connected to the VCC pin is charged via the startup resistor and the voltage increases. The IC is then in standby start and almost no current is consumed. ( $I_{CC} < 2\mu A$ ) Thereafter, VCC reaches the OFF threshold voltage of UVLO (VCCON) and the IC begins operation. When the IC begins operation to make output, the IC operates based on the voltage from the auxiliary winding. When the IC is just starting up, however, it takes time for the voltage from the auxiliary winding to rise enough, and VCC drops during this period.

Determine the VCC capacitor value so that VCC will not drop down to the ON threshold voltage of UVLO (VCCOFF) during this period. When the VCC capacitor is too small, VCC will drop down to the ON threshold voltage of UVLO before the auxiliary winding to rise. It becomes impossible to startup the power supply as VCC repeats the top and bottom between the VCCOFF and VCCON in this case (Fig.21).

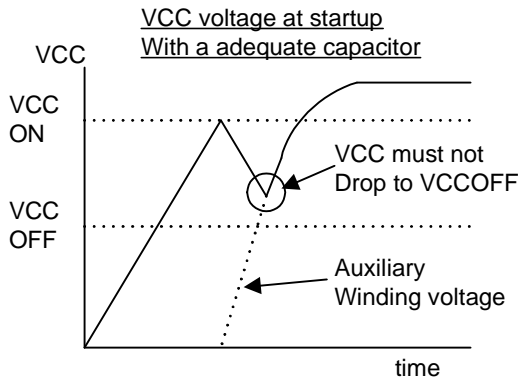


Fig.20

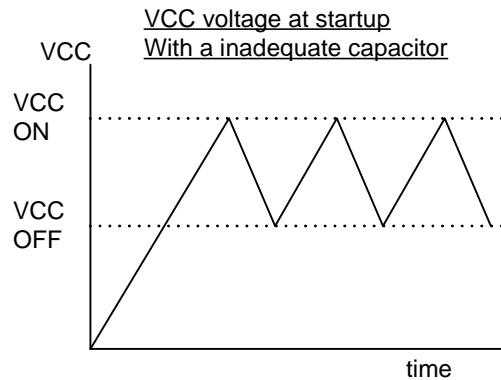


Fig.21

**(3)The startup period**

In the case of the circuit in Fig. 22 (R1: starting resistance), the starting time Tst [ms] until the IC is started after the power is turned on is determined by the following approximate formula:

$$T_{st} = -C2 \times R1 \times \ln\left(1 - \frac{17.5}{V1}\right) \dots\dots\dots(7)$$

In the case of the circuit in Fig. 23, the starting time Tst [ms] until the IC is started after the power is turned on is determined by the following approximate equation:

$$T_{st} = -C2 \times R0 \times \ln\left(1 - \frac{17.5}{V_{vcc}}\right) \dots\dots\dots(8) \quad R0 = \frac{R1 \cdot R2}{R1 + R2} \quad V_{vcc} = \frac{R2}{R1 + R2} \times V1$$

$$V1 = \begin{cases} \frac{\sqrt{2} \times Vac}{\pi} \dots\dots \text{(If the starting resistor is before rectification)} \dots\dots\dots(9) \\ \sqrt{2} \times Vac \dots\dots \text{(If the starting resistor is after rectification)} \dots\dots\dots(10) \end{cases}$$

Where, R1: starting resistance [kΩ], C2: the capacitor between the VCC and the GND [μF], Vac: an effective value of the AC input voltage [V]

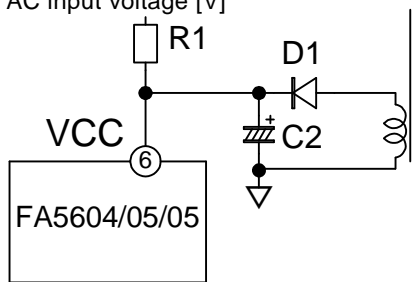


Fig.22

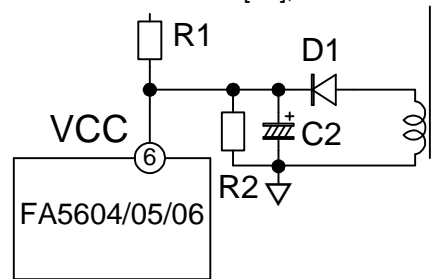


Fig.23

The above formulas are intended for approximate calculation of the starting time. Please note that the calculation results may not actually be the same as measured values because of the startup current or the like.

To shorten the startup period, the capacitor C2 or resistor R1 should be decreased. But in some case, such as when the load current of the power supply is changed rapidly, you may want to prolong the hold time of the VCC voltage over the VCC the OFF threshold. In this case, the capacitor C2 cannot be decreased and the resistor R1 should be decreased. But loss of the resistor R1 increases. In such case, the circuit shown in **Fig.24** and **Fig.25** is effective to shorten startup period without increasing the loss of the resistor R1. The capacitor C2 is decreased to shorten the startup period and, after the IC startup, VCC voltage supplied from C3 to prolong the hold time of the VCC voltage. The startup period of this circuit also is approximately given by the expression in (7) and (8).

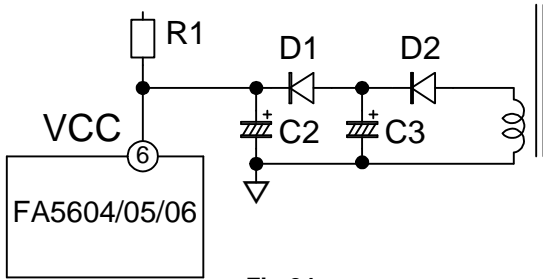


Fig.24

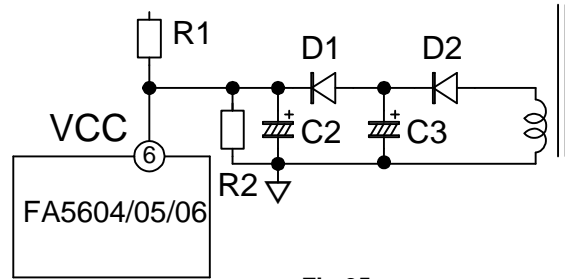


Fig.25

**(4)Feedback pin circuit**

**Fig.26** shows an example of connection in which a feedback signal is input to the FB pin. If this circuit causes power supply instability, connect R3 and C4 as shown in **Fig.26** to decrease the frequency gain. Set R3 between several 10Ω to several kΩ and C4 between several 100pF to 1μF.

In noise is applied to the FB pin, the output pulses may be lacked or disturbed.

In this case, connect a capacitor C5 as shown in **Fig.26** to suppress the noise applied to the FB pin. Set the capacitor of C5 less than 1/10 of capacitance of C4 and connect C5 as near the IC as possible.

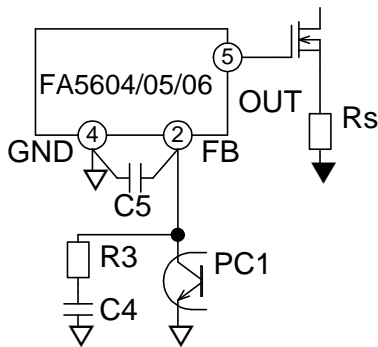


Fig.26

**(5)The correct overcurrent limiting protection**

The output power at overvoltage is limited by the overcurrent limiting function of the IC. However, in general, the characteristics that the voltage is reduced while the current is increased is shown as indicated in “(1) Not corrected” in Fig. 27.

For this IC, as shown in Fig. 28, it is possible to correct the overcurrent limit in order to obtain the output characteristics like (2) by smoothing the OUT terminal voltage by R4 and C6 and apply it to the VF terminal for the forward circuit, or by applying the VCC voltage to the VF terminal for the flyback circuit. In addition, it is possible to obtain the output characteristics like (3) by adding R5 and D3 to correct it

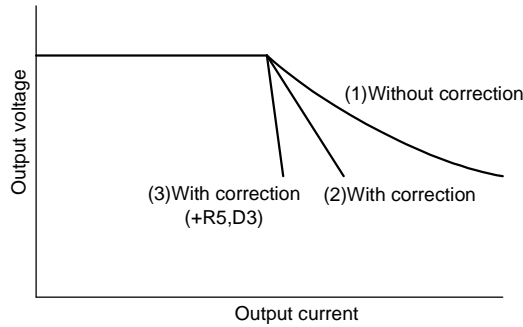


Fig.27

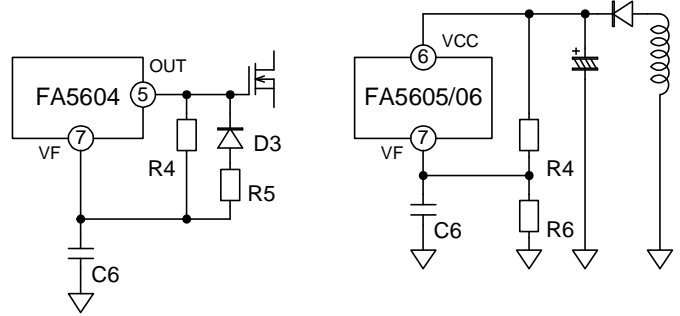


Fig.28

Note that if correcting the drooping characteristics at the power supply for which a hiccup operation is used, the power supply may not start because a hiccup operation is started at the startup depending on the CS terminal capacity (soft start) and the drooping correction constant (Fig. 29).

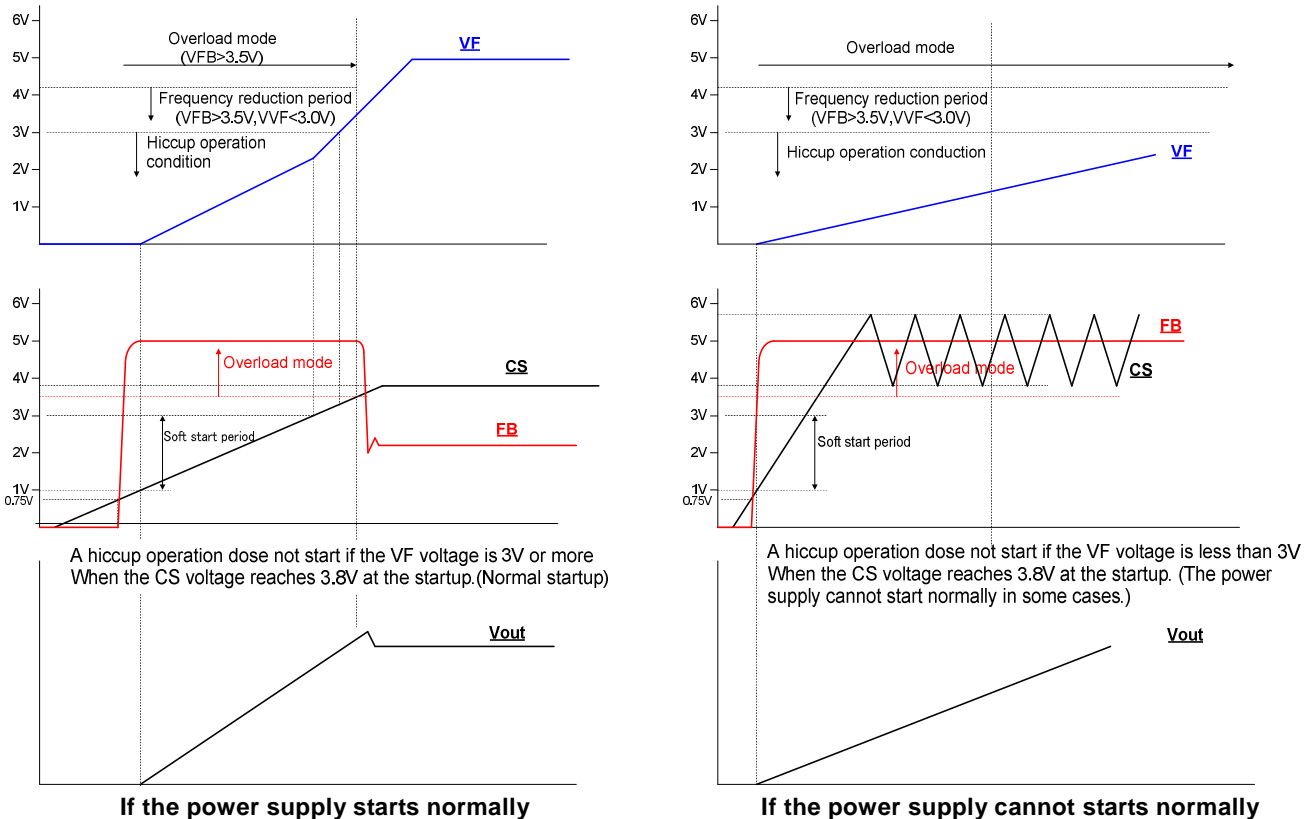


Fig.29

Because this IC adopts the frequency reduction method in which only the off period is extended, if the frequency is reduced at overload, the ON duty is also reduced, and therefore the output voltage is reduced. Consequently, the load current is reduced at the point in which it enters the drooping characteristics at overload (see Fig. 5 on p. 16).

**(6) Preventing malfunction caused by noise**

Noise applied to each pin may cause malfunction of the IC. If noise causes malfunction, see the notes summarized below and confirm in actual circuit to prevent malfunction.

- ① The IS pin for overcurrent limiting function detects the MOSFET current converted to the voltage. The parasitic capacitor and inductor of the MOSFET, transformer, wiring, etc. cause a noise in switching operation. If this switching noise causes a malfunction of overcurrent limiting function, insert the RC filter into IS pin as shown in Fig.13. Connect this capacitor as near the IC as possible to suppress noise effectively.
- ② If noise is applied to the FB pin, the output pulses may be disturbed. In this case, see .item (4) in Design advice.
- ③ Relatively large noise may occur at the VCC pin because large current flows from VCC pin to drive the MOSFET. Then noise may cause malfunction of the IC. In addition, the IC may stop operation when VCC voltage drops below the off threshold voltage by noise. Mind that capacitance and characteristics of the capacitor connected between VCC and GND pin not to allow the large noise at the VCC pin. To prevent malfunction, connect several 10μF electrolytic capacitor and about 0.1μF ceramic capacitor as near the IC as possible to suppress noise effective (Connect the ceramic capacitor nearer the IC than the electrolytic capacitor by priority).
- ④ RT terminal may cause a malfunction. It is recommended to install a capacitor of about 100 pF between the RT terminal and the GND. The line regulation may also be improved by this measure.

**(7) Preventing malfunction caused by negative voltage applied to a pin**

When large negative voltage is applied to each IC pin, a parasitic element in the IC may operate and cause malfunction. Be careful not allow the voltage applied to each pin to drop below -0.3V.

Especially for the OUT pin, voltage oscillation caused after the MOSFET turns off may be applied to the OUT pin via the parasitic capacitance of the MOSFET, causing the negative voltage to be applied to the OUT pin. If the voltage falls below -0.3V, add a Schottky diode between the OUT pin and the ground as shown in Fig.30.

The forward voltage of the Schottky diode can suppress the voltage applied to the OUT pin.

Use the low forward voltage of the Schottky diode.

Similarly, be careful not to cause the voltages at other pins fall below -0.3V.

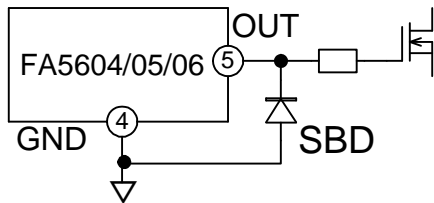


Fig.30

**(8) Gate circuit configuration**

To adjust switching speeds or prevent oscillation at gate terminals, resistors are normally inserted between the power MOSFET gate terminal to be driven and the OUT pin of the IC.

You may prefer to decide on the drive current independently, to turn the MOSFET on and off.

If so, connect the MOSFET gate terminal to the OUT pin of the IC as shown in Fig.31.

In this circuit, Rg1 and Rg2 restrict the current when the MOSFET is turned on, and only Rg1 restricts the current when it is turned off.

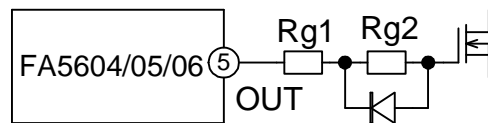


Fig.31

**(9) External latch (overvoltage protection on secondary side)**

Fig.32 shows the overvoltage shutdown circuit based on the signal from the secondary side.

The optocoupler output transistor is connected between the CS and VCC pins. When the output voltage is put in the overvoltage state, the optocoupler output transistor goes on to raise the CS pin voltage via resistor R2. When the CS pin voltage exceeds the reference voltage (7.3V) of internal comparator, the IC enters the OFF latch mode and shuts the output down. The IC consumes current 190µA (typ.) (VCC=14V) in latch mode. This circuit must be supplied via startup resistor R1. The overvoltage protection circuit can be reset by lowering the supply voltage VCC to below 9.7V or forcing the CS pin voltage below 7.3V.

In normal operation, the CS pin voltage is clamped by the 3.8V zener diode with maximum sink current 100µA (max.). Therefore, to raise the CS pin voltage to 7.3V or more, 200µA or a higher current needs to be supplied from the optocoupler. Set the current input to the CS pin to 2mA or less.

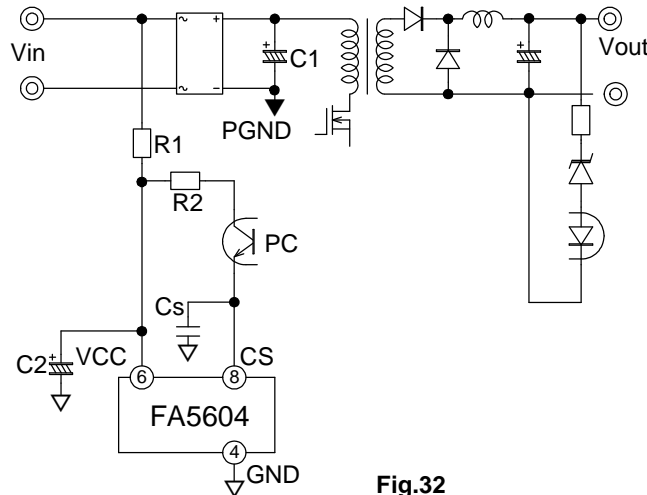


Fig.32

**(10) Not used the overload shutdown function**

As explained by pre-block (6), the clamp CS pin voltage (3.8V) is canceled at overload (VFB>3.5V, VVF<3V), and the CS pin voltage oscillates and counts between 3.8V and 5.7V. The overload shutdown function is prevented by clamping the CS pin voltage on the outside.

Fig.33 shows the CS pin voltage is clamped by internal zener diode ZD. In this case, because of zener current Iz is 10 µA, please set the zener voltage to between 3.8V to 5.7V.

$$V_{CS} = V_z = 3.8V \text{ to } 5.7V \quad \dots\dots\dots (11)$$

Moreover, when the overvoltage protection function is made effective, you set external pull-up to exceed the latch threshold voltage 7.3V by using the zener diode ZD and the resistor R (Fig.28). In that case, the zener voltage Vz should consider the voltage (R×Iz) of the resistor R.

$$V_{CS} = V_z + (R \times I_z) = 3.8V \text{ to } 5.7V \quad \dots\dots\dots (12)$$

When the IC operate of overvoltage protection, to raise the CS pin voltage to 7.3V or more, 200µA to 2mA current needs to be supplied. In this case, because the zener current Izovp (1mA etc) differs from Iz=10µA, the zener voltage Vzovp differs from Vz.

$$V_{CS} = V_{zovp} + (R \times I_{zovp}) \geq 7.3V \quad \dots\dots\dots (13)$$

Because a method in which the VF pin is not reduced to less than 3 V interferes with reduction of the frequency, it is recommended to use a method in which the CS pin is clamped by the Zener diode.

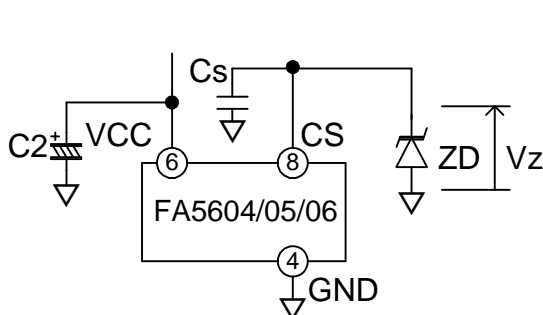


Fig.33

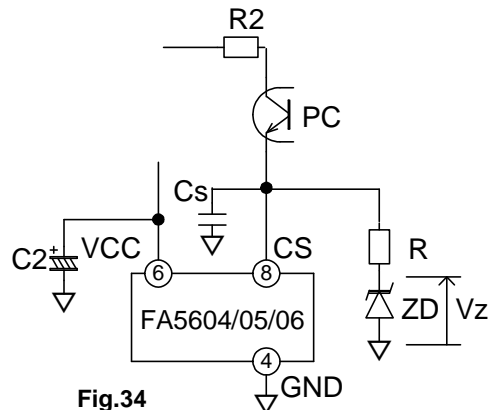


Fig.34

**(11) Loss calculation**

IC loss must be confirmed to use the IC within the ratings.

Since it is hard to directly measure IC loss, some examples of calculating approximate IC loss are given below.

**(11-1) Calculation example 1**

Suppose the supply voltage is VCC, IC current consumption is ICC, the total gate charge of the power MOSFET is Qg, and the switching frequency is fosc. Total IC loss Pd can be calculated by:

$$Pd \approx VCC \times (ICC + Qg \times fosc) \quad \dots\dots\dots (14)$$

This expression calculates an approximate value of Pd, which is normally a little larger than the actual loss. Since various conditions such as temperature characteristics apply, thoroughly verify the appropriateness of the calculation under all applicable conditions.

**Example:**

When VCC=18V, ICC=3mA (max.) is obtained from the specifications. Suppose Qg=80nC and fosc=190kHz.

$$Pd \approx 18V \times (3mA + 80nC \times 190kHz) \approx 328mW$$

**(11-2) Calculation example 2**

The IC loss consists of the loss caused by operation of the control circuit and the loss caused at the output circuit to drive the power MOSFET.

**① Loss at the control circuit**

The loss caused by operation of the IC control circuit is calculated by the supply voltage and IC current consumption. When the supply voltage is VCC and IC current consumption is ICC, loss Pcon at the control circuit is:

$$Pcon = VCC \times ICC \quad \dots\dots\dots (15)$$

**Example:**

When VCC=18V, ICC=1.6mA (max.) is obtained from the specifications. The typical IC loss is given by:

$$Pcon = 18V \times 1.6mA \approx 29mW$$

**② Loss at the output circuit**

The output circuit of the IC is a MOSFET push-pull circuit. When the ON resistances of MOSFETs making up the output circuit are Ron and Roff, the resistances can be determined as shown below based on VCC=18V obtained from the output characteristics shown in the specifications:

$$Ron = 15\Omega \text{ (typ)}, \quad Roff = 7\Omega \text{ (typ)}$$

When the total gate charge of the power MOSFET is Qg, the switching frequency is fosc, the supply voltage is VCC and gate resistance is Rg, the loss (Pdr) caused at the IC output circuit is given by:

$$Pdr = \frac{1}{2} \times VCC \times Qg \times fosc \times \left( \frac{Ron}{Rg + Ron} + \frac{Roff}{Rg + Roff} \right) \quad \dots\dots\dots (16)$$

When gate resistance differs between ON and OFF as shown in **Fig.31**, the loss is given by:

$$Pdr = \frac{1}{2} \times VCC \times Qg \times fosc \times \left( \frac{Ron}{Rg1 + Rg2 + Ron} + \frac{Roff}{Rg1 + Roff} \right) \quad \dots\dots\dots (17)$$

**Example:**

When VCC=18V, Qg=80nC, fosc=190 kHz and Rg=10Ω, the typical IC loss is given by:

$$Pdr = \frac{1}{2} \times 18V \times 80nC \times 190kHz \times \left( \frac{15\Omega}{10\Omega + 15\Omega} + \frac{7\Omega}{10\Omega + 7\Omega} \right) = 138mW$$

**Total loss**

The total loss (Pd) of the IC is the sum of the control circuit loss (Pcon) and the output circuit loss (Pdr) calculated previously:

$$Pd = Pcon + Pdr \quad \dots\dots\dots (18)$$

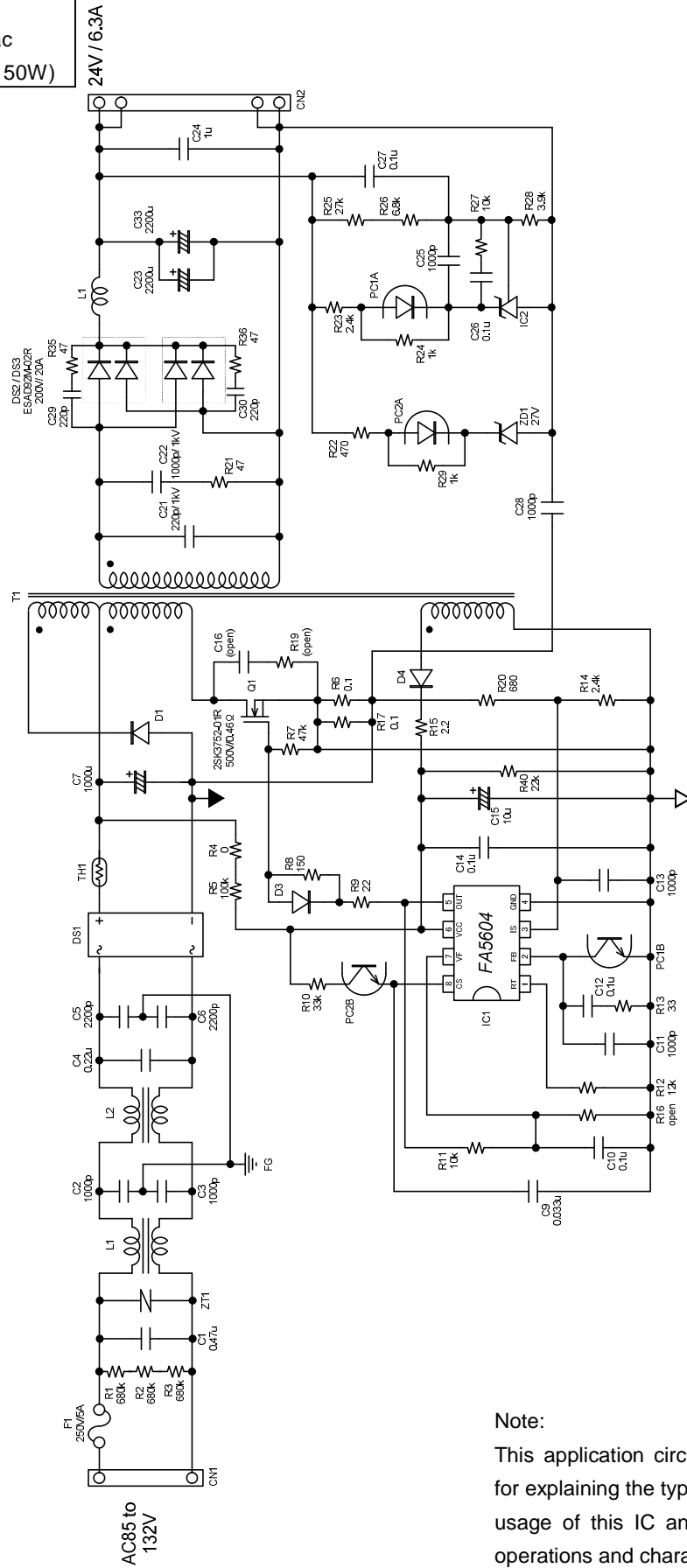
**Example:**

The standard IC loss under the conditions used in ① and ② above are:

$$Pd = Pcon + Pdr = 29mW + 138mW = 167mW$$

**11 .Application circuit**

- Forward
- Input ; 85Vac to 132Vac
- Output ; 24Vdc,6.3A (150W)



**Note:**  
 This application circuit example is a reference for explaining the typical usage of this IC and does not guarantee the operations and characteristics.