IXDN404PI / N404SI / N404SI-16 IXDI404PI / I404SI / I404SI-16 IXDF404PI / F404SI / F404SI-16

4 Ampere Dual Low-Side Ultrafast MOSFET Drivers

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected Over Entire Operating Range
- High Peak Output Current: 4A Peak
- Wide Operating Range: 4.5V to 25V
- High Capacitive Load Drive Capability: 1800pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two Drivers in Single Chip

Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Limiting di/dt Under Short Circuit

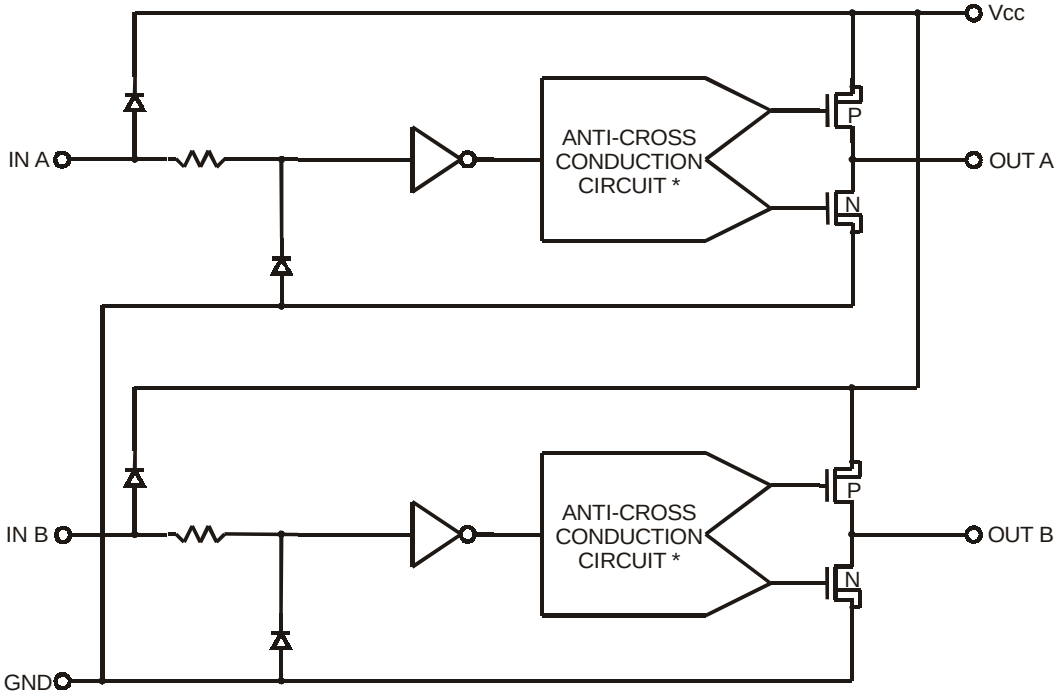
General Description

The IXDN404/IXDI404/IXDF404 is comprised of two 4 Ampere CMOS high speed MOSFET drivers. Each output can source and sink 4A of peak current while producing voltage rise and fall times of less than 15ns to drive the latest IXYS MOSFETs & IGBT's. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. A patent-pending circuit virtually eliminates CMOS power supply cross conduction and current shoot-through. Improved speed and drive capabilities are further enhanced by very low, matched rise and fall times.

The IXDN404 is configured as a dual non-inverting gate driver, the IXDI404 is a dual inverting gate driver, and the IXDF404 is a dual inverting + non-inverting gate driver.

The IXDN404/IXDI404/IXDF404 family are available in the standard 8 pin P-DIP (PI), SOP-8 (SI) and SOP-16 (SI-16) packages.

Figure 1 - IXDN404 Dual 4A Non-Inverting Gate Driver Functional Block Diagram



* Patent Pending

Figure 2 - IXDI404 Dual Inverting 4A Gate Driver Functional Block Diagram

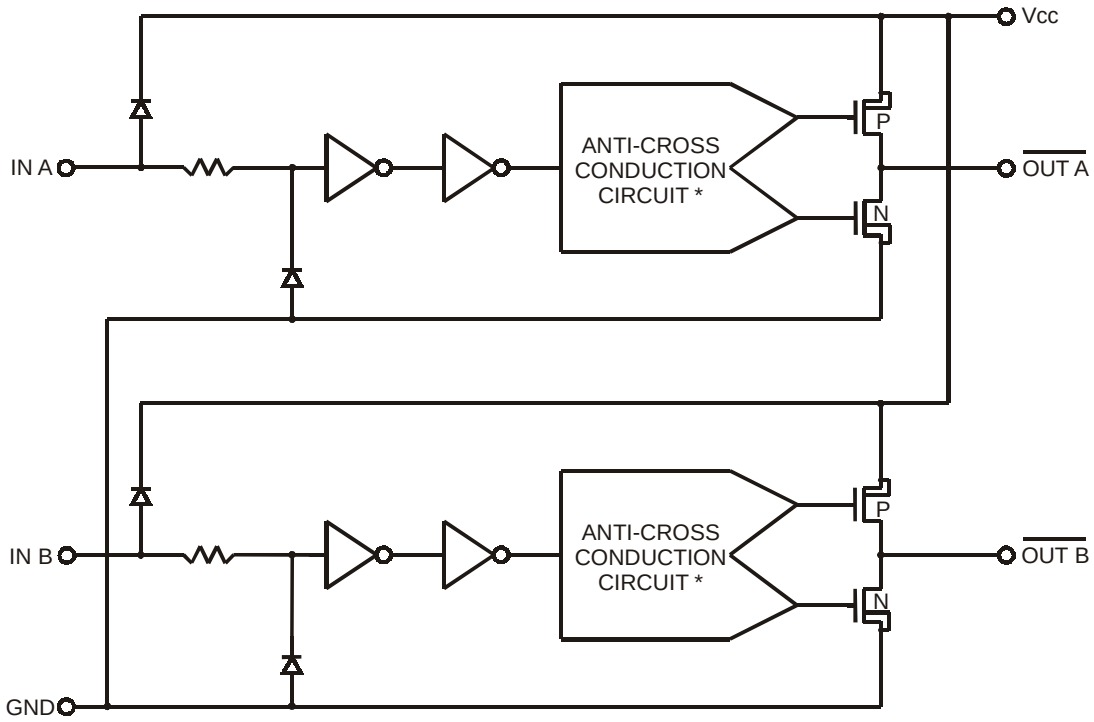
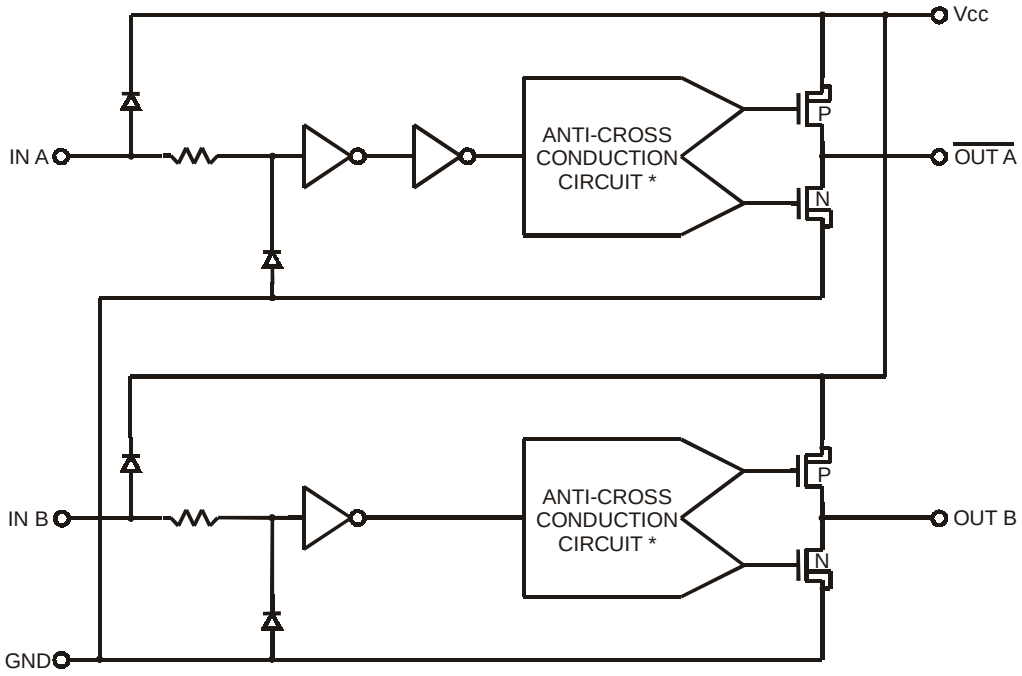


Figure 3 - IXDF404 Inverting + Non-Inverting 4A Gate Driver Functional Block Diagram



* Patent Pending

Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	25V
All Other Pins	-0.3V to V_{CC} + 0.3V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C

Operating Ratings

Parameter	Value
Operating Temperature Range	-40°C to 85°C
Thermal Impedance (Junction To Ambient)	
8 Pin PDIP (PI) (θ_{JA})	120°C/W
8 Pin SOIC (SI) (θ_{JA})	110°C/W
16 Pin SOIC (SI-16) (θ_{JA})	110°C/W

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 4.5V ≤ V_{CC} ≤ 25V .
All voltage measurements with respect to GND. Device configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		3.5			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output High	I_{OUT} = 10mA, V_{CC} = 18V		1.5	3	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 18V		1.5	3	Ω
I_{PEAK}	Peak output current	V_{CC} is 18V		4		A
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_L=1800pF Vcc=18V	11	12	15	ns
t_F	Fall time	C_L=1800pF Vcc=18V	12	14	17	ns
t_{ONDLY}	On-time propagation delay	C_L=1800pF Vcc=18V	33	34	38	ns
t_{OFFDLY}	Off-time propagation delay	C_L=1800pF Vcc=18V	28	30	35	ns
V_{CC}	Power supply voltage		4.5	18	25	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Ordering Information

Part Number	Package Type	Temp. Range	Configuration
IXDN404PI	8-Pin PDIP	-40°C to +85°C	Dual Non Inverting
IXDN404SI	8-Pin SOIC		
IXDN404SI-16	16-Pin SOIC		
IXDI404PI	8-Pin PDIP	-40°C to +85°C	Dual Inverting
IXDI404SI	8-Pin SOIC		
IXDI404SI-16	16-Pin SOIC		
IXDF404PI	8-Pin PDIP	-40°C to +85°C	Inverting + Non Inverting
IXDF404SI	8-Pin SOIC		
IXDF404SI-16	16-Pin SOIC		

NOTE: Mounting or solder tabs on all packages are connected to ground

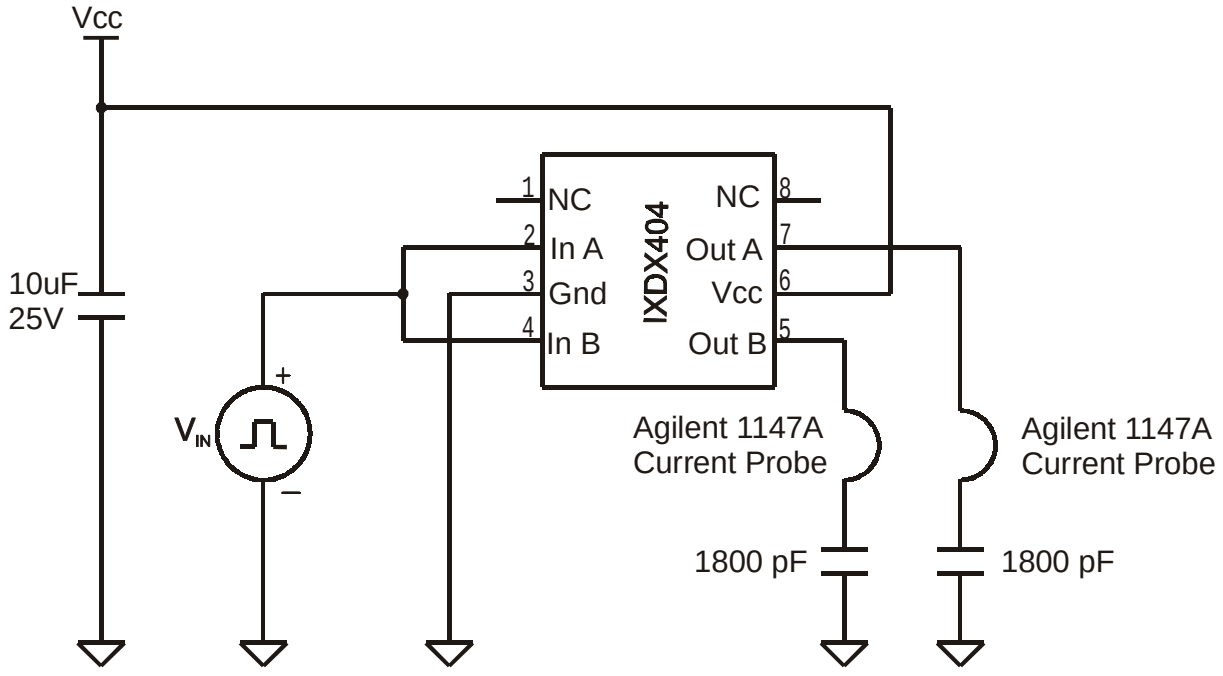
Pin Description

SYMBOL	FUNCTION	DESCRIPTION
IN A	A Channel Input	A Channel Input signal-TTL or CMOS compatible.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
IN B	B Channel Input	B Channel Input signal-TTL or CMOS compatible.
OUT B	B Channel Output	B Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 25V.
OUT A	A Channel Output	A Channel Driver output. For application purposes, this pin is connected via a resistor to a gate of a MOSFET/IGBT.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Note 1: Operating the device beyond parameters with listed "Absolute Maximum Ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Figure 4 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 5 Rise Time vs. Supply Voltage

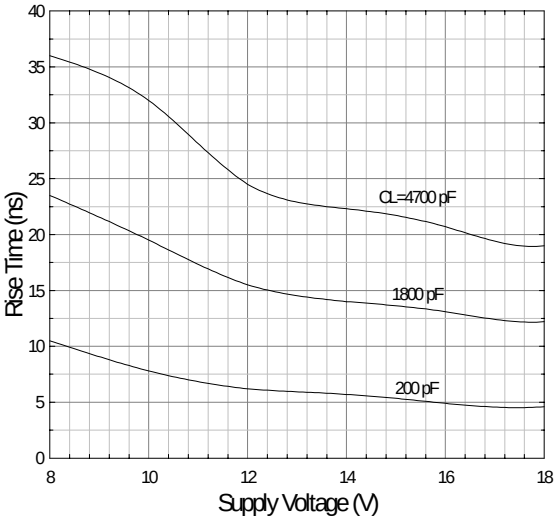


Fig. 6 Fall Time vs. Supply Voltage

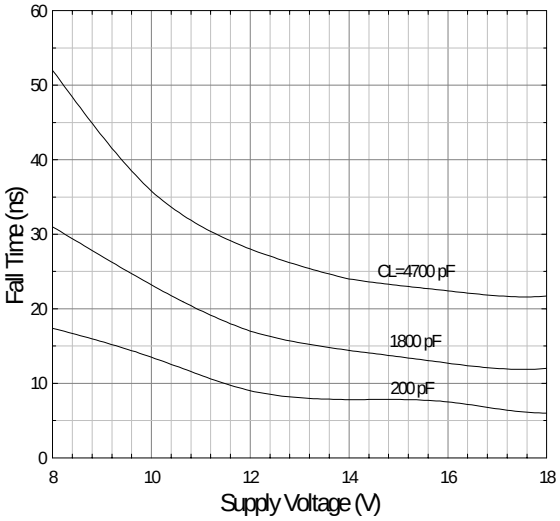


Fig. 7 Rise And Fall Times vs. Case Temperature
C_L=1nF V_{CC}=18V

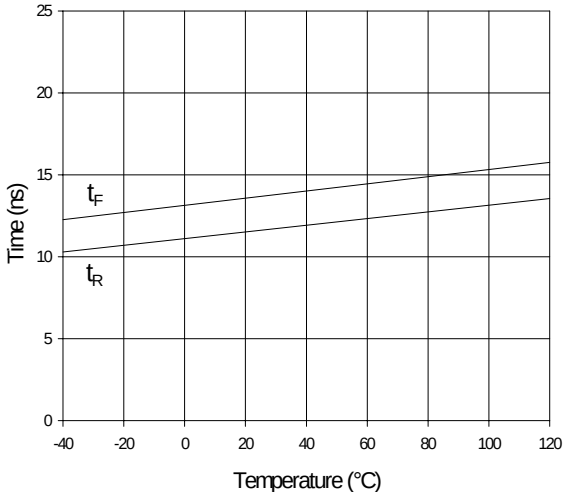


Fig. 8 Rise Time vs. Load Capacitance

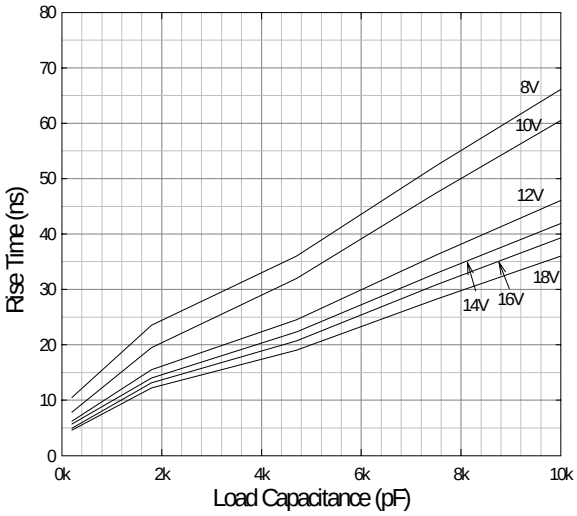


Fig. 9 Fall Time vs. Load Capacitance

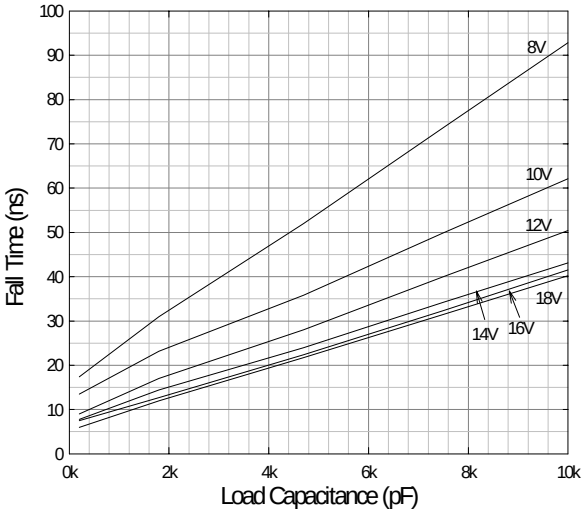


Fig. 10 Max / Min Input vs. Case Temperature
V_{CC}=18V C_L=1nF

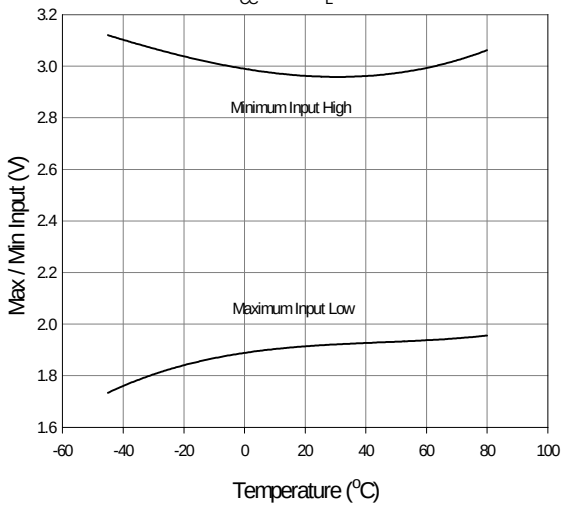


Fig. 11 Supply Current vs. Load Capacitance Vcc=18V

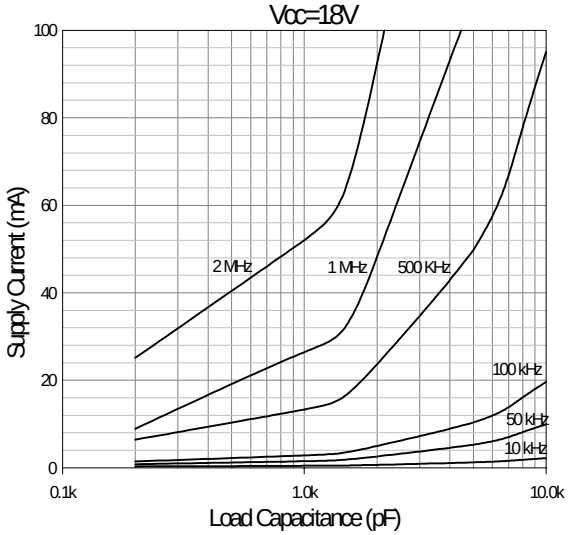


Fig. 12 Supply Current vs. Frequency Vcc=18V

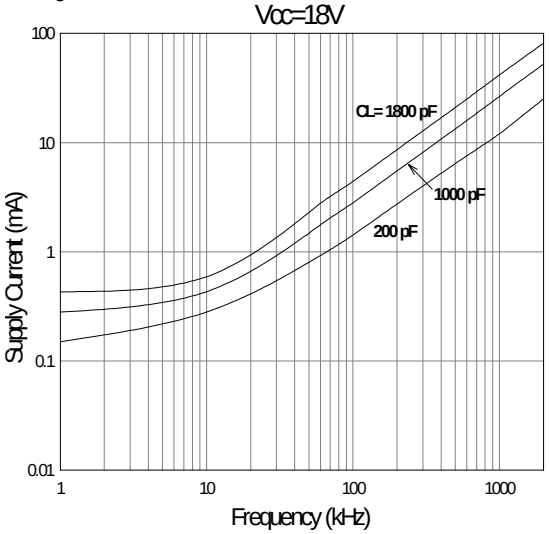


Fig. 13 Supply Current vs. Load Capacitance Vcc=12V

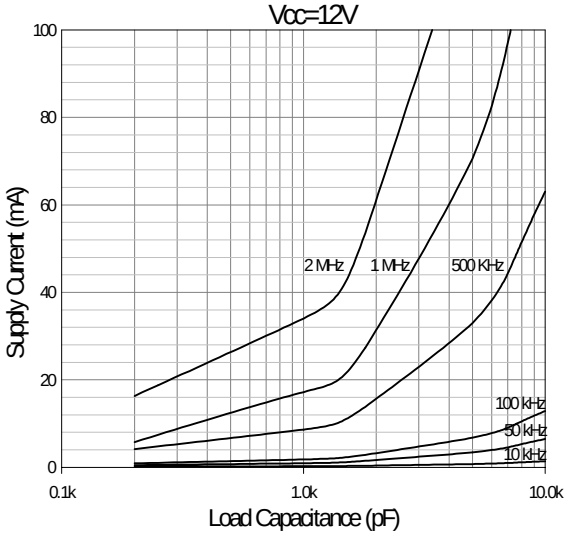


Fig. 14 Supply Current vs. Frequency Vcc=12V

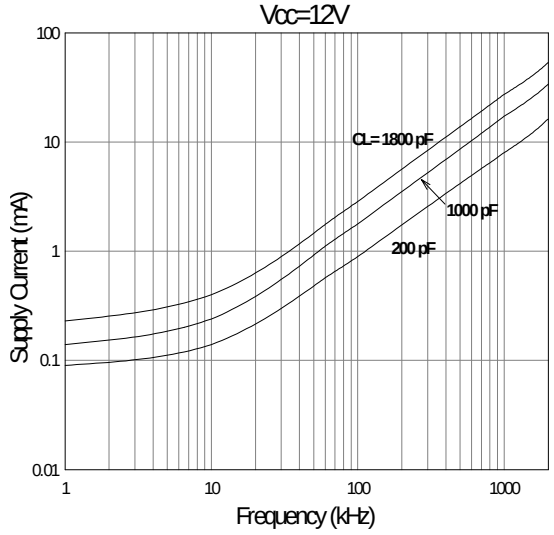


Fig. 15 Supply Current vs. Load Capacitance Vcc=8V

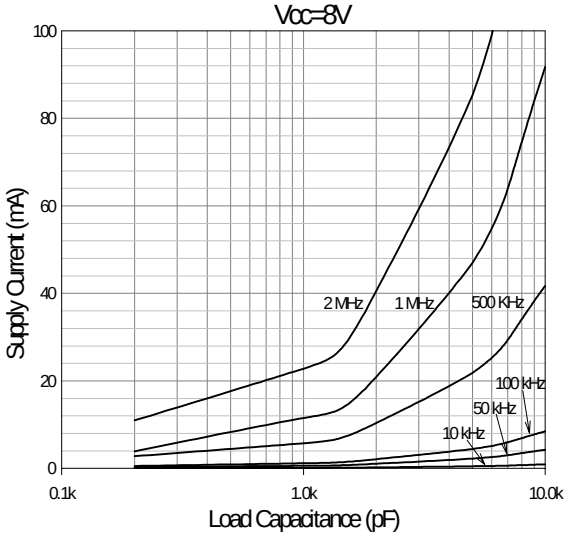


Fig. 16 Supply Current vs. Frequency Vcc=8V

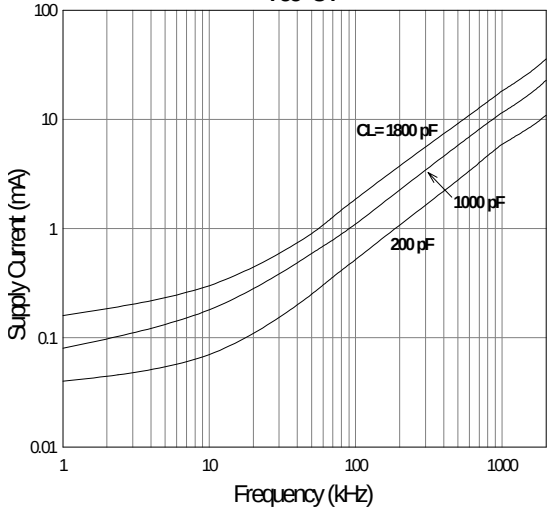


Fig. 17 Propagation Delay vs. Supply Voltage
C_L=1800pF V_{IN}=5V@1kHz

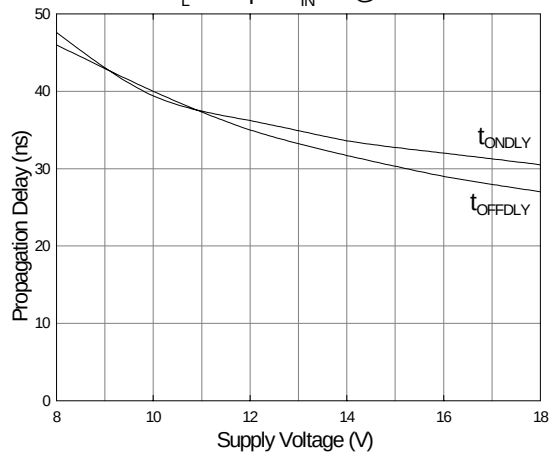


Fig. 18 Propagation Delay vs. Input Voltage
C_L=1800pF V_{CC}=15V

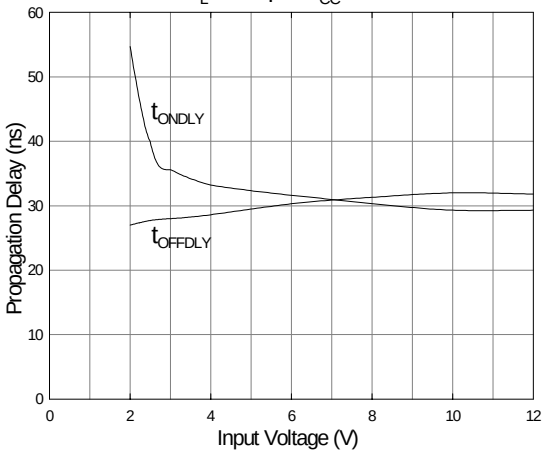


Fig. 19 Propagation Delay Times vs. Temperature
C_L=1800pF V_{CC}=18V

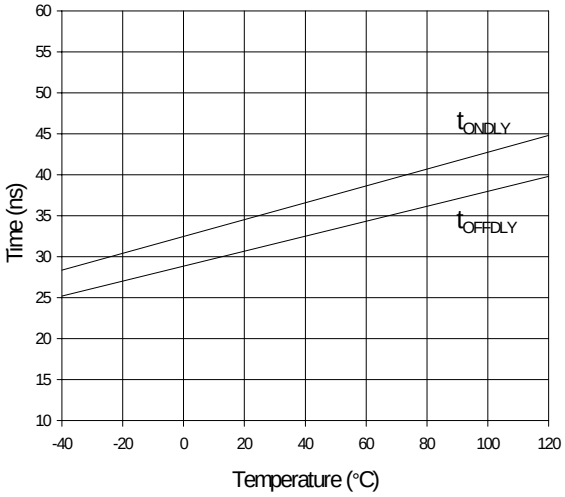


Fig. 20 Quiescent Supply Current vs. Temperature
V_{CC}=18V V_{IN}=5V@1kHz C_L=1000pF

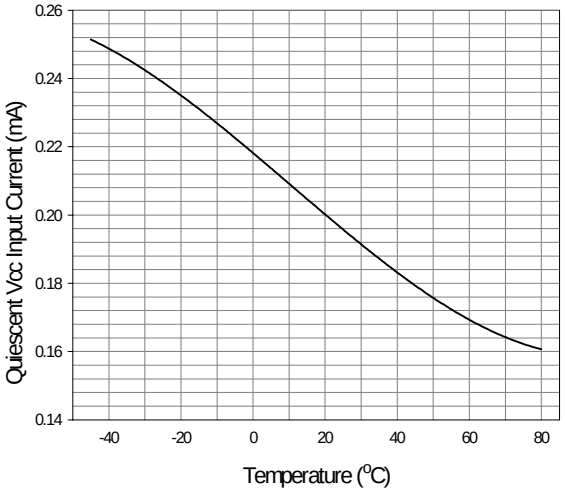


Fig. 21 P Channel Output Current Vs. Temperature
V_{CC}=18V, C_L=1000pF

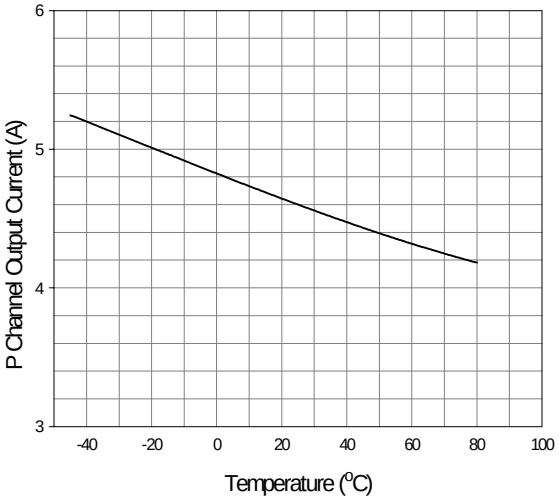


Fig. 22 N Channel Output Current Vs. Temperature
V_{CC}=18V, C_L=1000pF

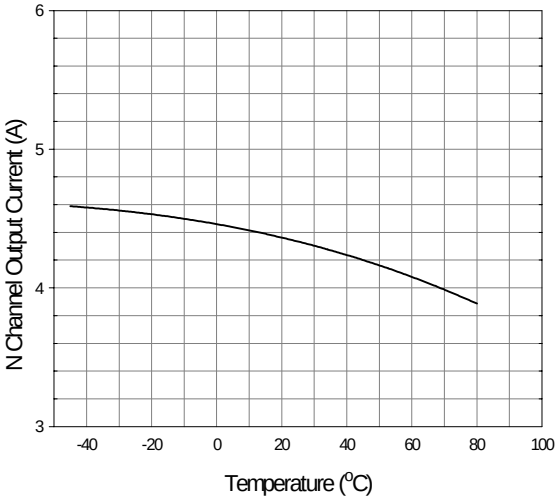


Fig. 23 High State Output Resistance vs. Supply Voltage

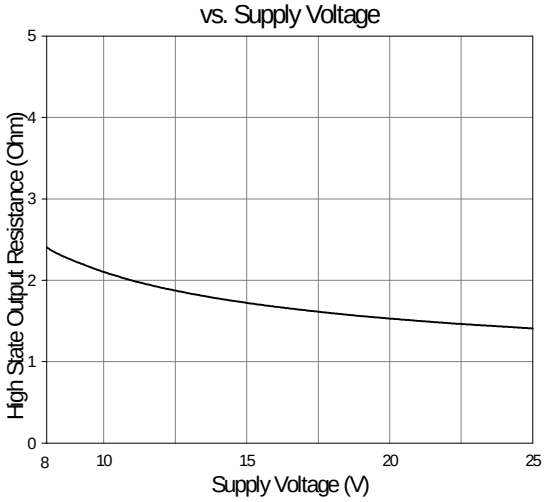


Fig. 24 Low-State Output Resistance Vs. Supply Voltage

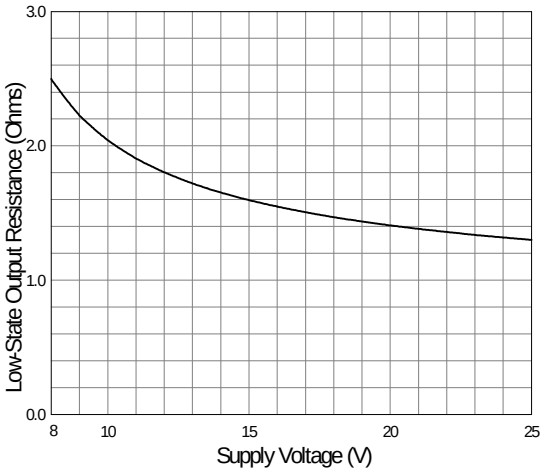


Fig. 25 V_{cc} vs. P Channel Output Current

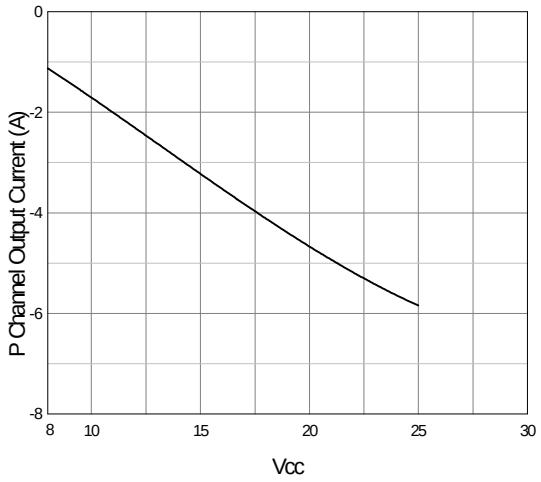
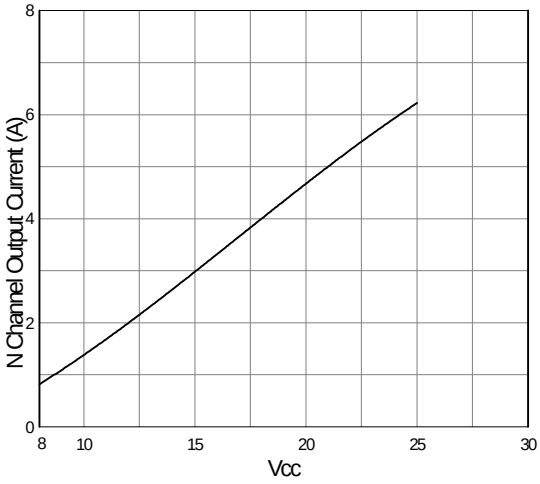
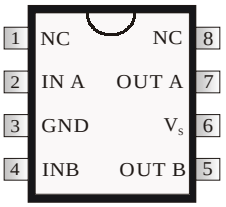


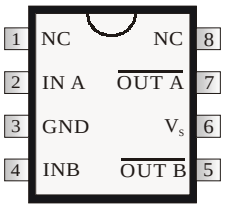
Fig. 26 V_{CC} vs. N Channel Output Current



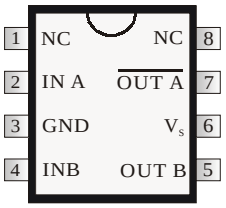
PIN CONFIGURATIONS



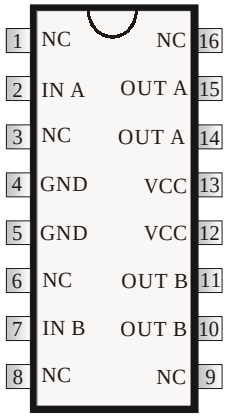
8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDN404



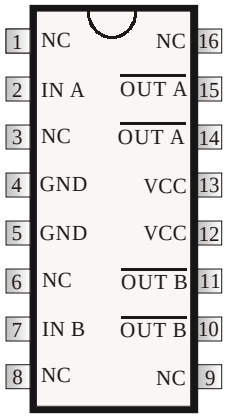
8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDI404



8 Lead PDIP (PI)
8 Pin SOIC (SI)
IXDF404



16 Pin SOIC
IXDN404SI-16



16 Pin SOIC
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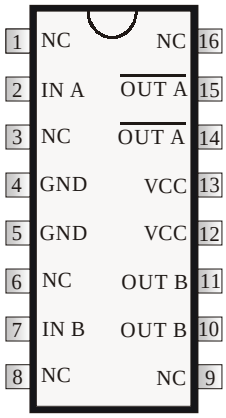


16 Pin SOIC
IXDF404SI-16

Supply Bypassing, Grounding Practices And Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDN404/IXDI404/IXDF404, it is very important to observe certain design criteria in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDN404 to charge a 2500pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I = \Delta V\ C / \Delta t$, where ΔV=25V C=2500pF & Δt=25ns, we can determine that to charge 2500pF to 25 volts in 25ns will take a constant current of 2.5A. (In reality, the charging current won't be constant, and will peak somewhere around 4A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDN404 must be able to draw this 2.5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDN404 to an absolute minimum.

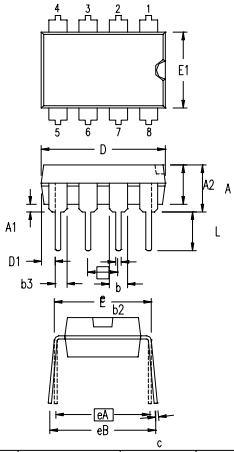
GROUNDING

In order for the design to turn the load off properly, the IXDN404 must be able to drain this 2.5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDN404 and its load. Path #2 is between the IXDN404 and its power supply. Path #3 is between the IXDN404 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDN404.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible. If the driver must be placed farther than 2" (5mm) from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connected directly to the ground terminal of the load.

REV	DATE	ECN NO	DESCRIPTION	APR

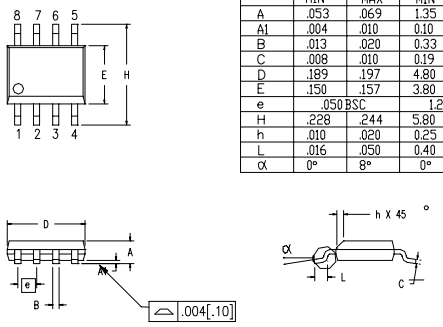


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

IXYS Corp 3540 Bassett St., Santa Clara, CA 95054	TOLERANCE Unless Otherwise Specified .X=+/-.05 .XXX=+/-.005 .XX=+/-.01 ANGLE=+/-5	DATE: 8/18/94	DWN: K. R. Choi	TITLE CASE OUTLINE OF 8 LEAD 0.3"W P-DIP	DRAWING NO CO 0035	REV 0
		UNIT: INCH [MM]	APR:			
		SACLE: 4 X	APR:			

REV	DATE	ECN NO	DESCRIPTION	APR

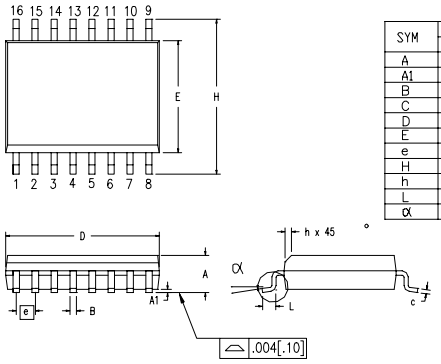


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

IXYS Corp 3540 Bassett St., Santa Clara, CA 95054	TOLERANCE Unless Otherwise Specified .X=+/-.05 .XXX=+/-.005 .XX=+/-.01 ANGLE=+/-5	DATE: 1/24/95	DWN: K. R. Choi	TITLE CASE OUTLINE SOP-8 (.150"W)	DRAWING NO CO 0044	REV 0
		UNIT: INCH [MM]	APR:			
		SACLE: 5X	APR:			

REV	DATE	ECN NO	DESCRIPTION	APR



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-013 AA.

IXYS Corp 3540 Bassett St., Santa Clara, CA 95054	TOLERANCE Unless Otherwise Specified .X=+/-.05 .XXX=+/-.005 .XX=+/-.01 ANGLE=+/-5	DATE: 10/7/92	DWN: K. R. Choi	TITLE CASE OUTLINE SOP-16 (.300"W)	DRAWING NO CO 0016	REV 0
		UNIT: INCH [MM]	APR:			
		SACLE: 5X	APR:			

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