M51996AP/FP

SWITCHING REGULATOR CONTROL

DESCRIPTION

M51996A is the primary switching regulator controller which is especially designed to get the regulated DC voltage from AC power supply.

This IC can directly drive the MOS-FET with fast rise and fast fall output pulse and with a large-drive totempole output.

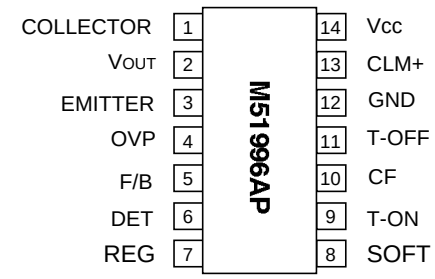
Type M51996A has the functions of not only high frequency OSC and fast output drive but also current limit with fast response and high sensibility so the true "fast switching regulator" can be realized.

The M51996A is equivalent to the M51978 with externally re-settable OVP(over voltage protection)circuit.

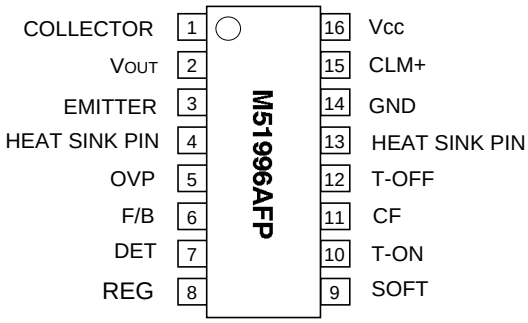
FEATURES

- 500kHz operation to MOS FET
- Output current.....±1A
- Output rise time 60ns,fall time 40ns
- Modified totempole output method with small through current
- Compact and light-weight power supply
  - •Small start-up current.....100μA typ.
  - •Big difference between "start-up voltage" and "stop voltage" makes the smoothing capacitor of the power input section small. Start-up threshold 16V,stop voltage 10V
  - •Packages with high power dissipation are used to with-stand the heat generated by the gate-drive current of MOS FET. 14-pin DIP,16-pin SOP 1.5W(at 25°C)
- Simplified peripheral circuit with protection circuit and built-in large-capacity totempole output
  - •High-speed current limiting circuit using pulse-by-pulse method(CLM+pin)
  - •Over-voltage protection circuit with an externally re-settable latch(OVP)
  - •Protection circuit for output miss action at low supply voltage(UVLO)
- High-performance and highly functional power supply
  - •Triangular wave oscillator for easy dead time setting
  - •SOFT start function by expanding period

PIN CONFIGURATION (TOP VIEW)



Outline 14P4



Outline 16P2N-A

Connect the heat sink pin to GND.

APPLICATION

Feed forward regulator,fly-back regulator

RECOMMENDED OPERATING CONDITIONS

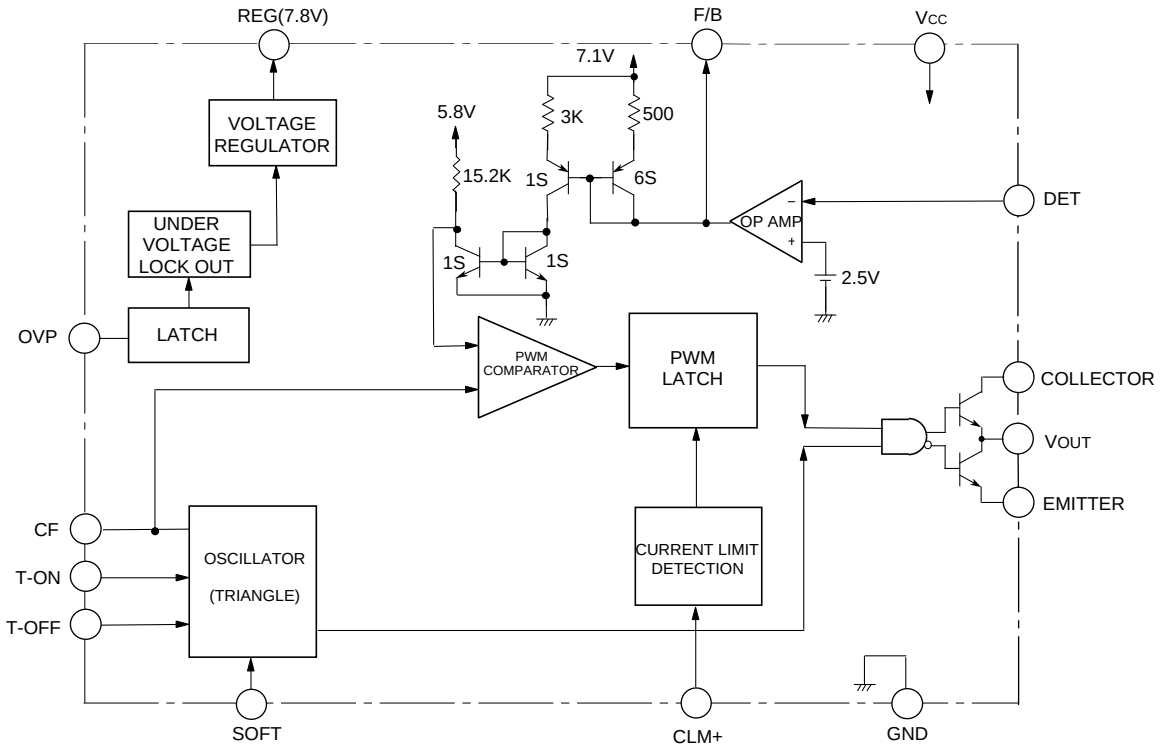
Supply voltage range.....12 to 30V

Operating frequency.....less than 500kHz

Oscillator frequency setting resistance

- •T-ON pin resistance RON.....10k to 75kΩ
- •T-OFF pin resistance ROFF.....2k to 30kΩ

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		31	V
V_C	Collector voltage		31	V
I_O	Output current	Peak	±1	A
		Continuous	±0.15	
I_{VREG}	V_{REG} terminal output current		-6	mA
V_{SOFT}	SOFT terminal voltage		V_{REG} +0.2	V
V_{CLM+}	CLM+ terminal voltage		-0.3 to +3	V
V_{DET}	DET terminal voltage		6	V
I_{OVP}	OVP terminal current		8	mA
I_{FB}	F/B terminal current		-10	mA
I_{TON}	T-ON terminal input current		-1	mA
I_{TOFF}	T-OFF terminal input current		-2	mA
P_d	Power dissipation	Ta=25˚C	1.5	W
K_θ	Thermal derating	Ta>25˚C	12	mW/˚C
T_{opr}	Operating temperature		-30 to +85	˚C
T_{stg}	Storage temperature		-40 to +125	˚C

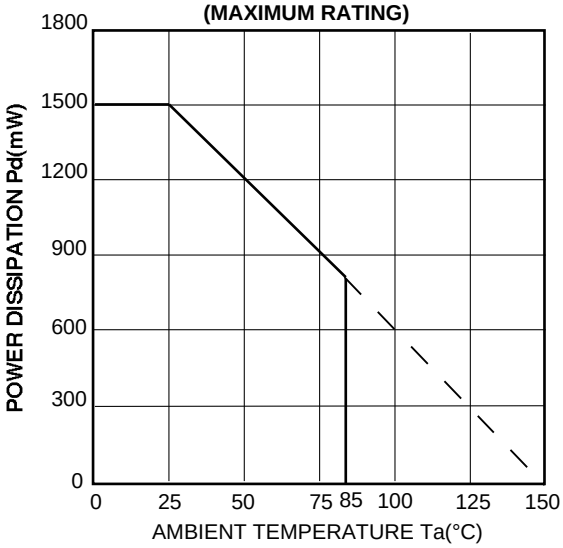
Note 1."+" sign shows the direction of current flowing into the IC and "-" sign shows the current flowing out from the IC.
2.The low impedance voltage supply should not be applied to the OVP terminal.

ELECTRICAL CHARACTERISTICS (V_{CC}=18V, Ta=25°C, unless otherwise noted)

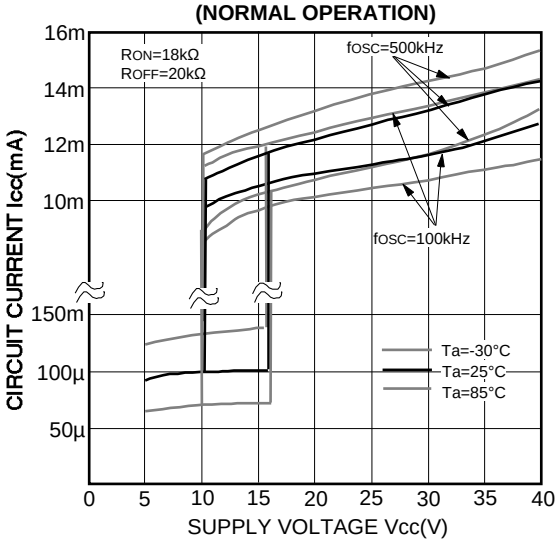
Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Supply voltage/circuit current	V_{CC}	Operating supply voltage range		$V_{CC(STOP)}$	—	30	V
	$V_{CC(START)}$	Operation start up voltage		15.2	16.2	17.2	V
	$V_{CC(STOP)}$	Operation stop voltage		9.0	9.9	10.9	V
	ΔVcc	$V_{CC(START)}$,$V_{CC(STOP)}$ difference	ΔVcc=$V_{CC(START)}$ -$V_{CC(STOP)}$	5.0	6.3	7.6	V
	I_{CCL}	Stand-by current	Vcc=14.5V,Ta=25°C	65	100	150	μA
			Vcc=14.5V,-30≤Ta≤85°C	50	100	200	
	I_{CCO}	Operating circuit current	Vcc=15V,f=188kHz	7.3	11	17	mA
			Vcc=30V,f=188kHz	8	12	19	
	I_{CCOVP}	Circuit current in OVP state	Vcc=25V	1.3	2.0	3.0	mA
			Vcc=9.5V	140	210	320	μA
F/B	I_{FBMIND}	Current at 0% duty	F/B terminal input current	-2.1	-1.5	-1.0	mA
	I_{FBMAXD}	Current at maximum duty	F/B terminal input current	-0.9	-0.6	-0.4	mA
	ΔI_{FB}	Current difference between max and 0% duty	ΔI_{FB}=I_{FBMIND}-I_{FBMAXD}	-1.35	-0.99	-0.70	mA
	V_{FB}	F/B terminal voltage	F/B terminal input current=0.95mA	4.9	5.9	7.1	V
	R_{FB}	OVP terminal resistance		420	600	780	Ω
OVP	V_{THOVPH}	OVP terminal H threshold voltage		540	750	960	mV
	ΔV_{THOVP}	OVP terminal hysteresis voltage	ΔV_{THOVP}=V_{THOVPH}-V_{THOVPL}		30		mV
	I_{THOVP}	OVP terminal threshold current		80	150	250	μA
	I_{INOVP}	OVP terminal input current	V_{OVP}=400mV	80	150	250	μA
	V_{CCOVPC}	OVP reset supply voltage	OVP terminal is open. (high impedance)	7.5	9.0	10.0	V
	$V_{CC(STOP)}$ -V_{CCOVPC}	Difference supply voltage between operation stop and OVP reset		0.55	1.20	—	V
	I_{THOVPC}	Current from OVP terminal for OVP reset	Vcc=30V	-480	-320	-213	μA
			Vcc=18V	-210	-140	-93	
CLM+	V_{THCLM+}	CLM+ terminal threshold voltage		180	200	220	mV
	I_{INCLM+}	CLM+ terminal current	V_{CLM+}=0V	-280	-200	-140	μA
	T_{PDCLM+}	Delay time from CLM+ to V_{OUT}		—	100	—	ns
Oscillator	f_{OSC}	Oscillating frequency	R_{ON}=20kΩ,R_{OFF}=17kΩ C_F=220pF,-5≤Ta≤85°C	170	188	207	kHz
	T_{DUTY}	Maximum ON duty		47	50	53	%
	V_{OSCH}	Upper limit voltage of oscillation waveform	R_{ON}=20kΩ,R_{OFF}=17kΩ C_F=220pF	3.97	4.37	4.77	V
	V_{OSCL}	Lower limit voltage of oscillation waveform		1.76	1.96	2.16	V
	ΔV_{OSC}	Voltage difference between upper limit and lower limit of OSC waveform		2.11	2.41	2.71	V
	V_{T-ON}	T-ON terminal voltage	R_{ON}=20kΩ	3.8	4.5	5.4	V
	V_{T-OFF}	T-OFF terminal voltage	R_{OFF}=17kΩ	2.9	3.5	4.2	V
SOFT	$f_{OSCSOFT}$	Oscillating frequency during SOFT operation (V_{SOFT}=5.5V)	R_{ON}=20kΩ,R_{OFF}=17kΩ C_F=220pF	170	188	207	kHz
		(V_{SOFT}=2.5V)		111	131	151	
		(V_{SOFT}=0.2V)		19.0	23.3	27.0	
	I_{SOFTIN}	SOFT terminal input current	V_{SOFT}=1V	-0.5	-0.1	—	μA
	I_{SOFDIS}	SOFT terminal discharging current	Discharge current of SOFT terminal at Vcc less than $V_{CC(STOP)}$	1	3.3	—	mA
REG	V_{REG}	Regulator output voltage		6.8	7.8	8.8	V
Output	V_{OL1}	Output low voltage	Vcc=18V,Io=10mA	—	0.04	0.4	V
	V_{OL2}		Vcc=18V,Io=100mA	—	0.7	1.4	V
	V_{OL3}		Vcc=5V,Io=1mA	—	0.85	1.0	V
	V_{OL4}		Vcc=5V,Io=100mA	—	1.3	2.0	V
	V_{OH1}	Output high voltage	Vcc=18V,Io=-10mA	16.0	16.7	—	V
	V_{OH2}		Vcc=18V,Io=-100mA	15.5	16.5	—	V
	T_{RISE}	Output voltage rise time		—	60	—	ns
	T_{FALL}	Output voltage fall time		—	40	—	ns
Detection	V_{DET}	Detection voltage		2.4	2.5	2.6	V
	I_{INDET}	DET terminal input current	V_{DET}=2.5V	—	1.0	3.0	μA
	G_{AVDET}	Voltage gain of detection amp		30	40	—	dB

TYPICAL CHARACTERISTICS

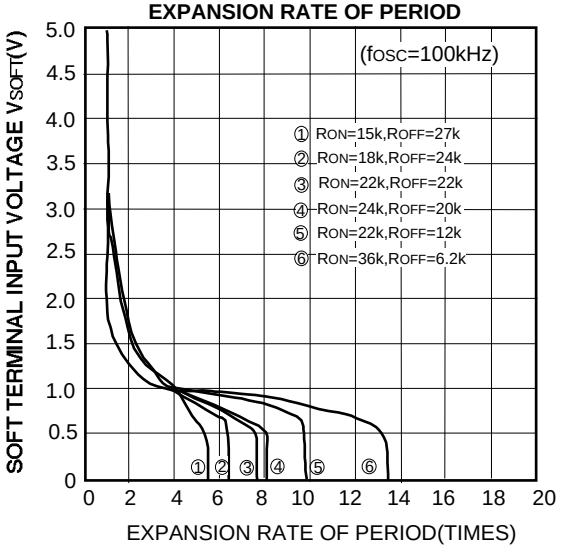
THERMAL DERATING
(MAXIMUM RATING)



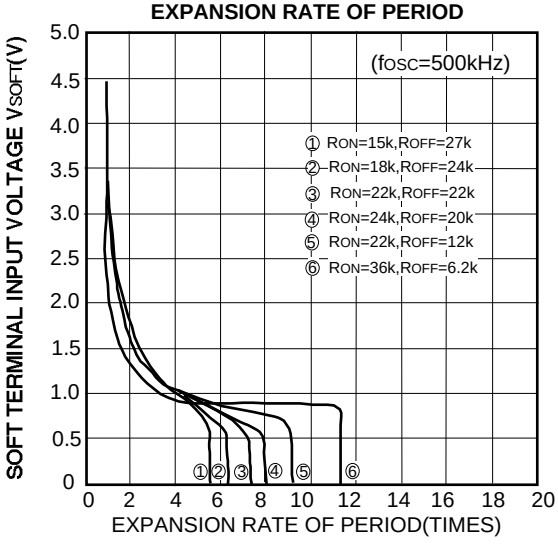
CIRCUIT CURRENT VS.SUPPLY VOLTAGE
(NORMAL OPERATION)



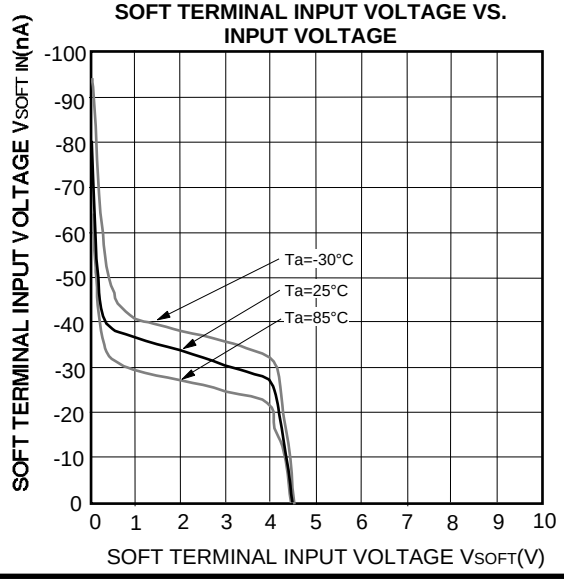
SOFT TERMINAL INPUT VOLTAGE VS.
EXPANSION RATE OF PERIOD



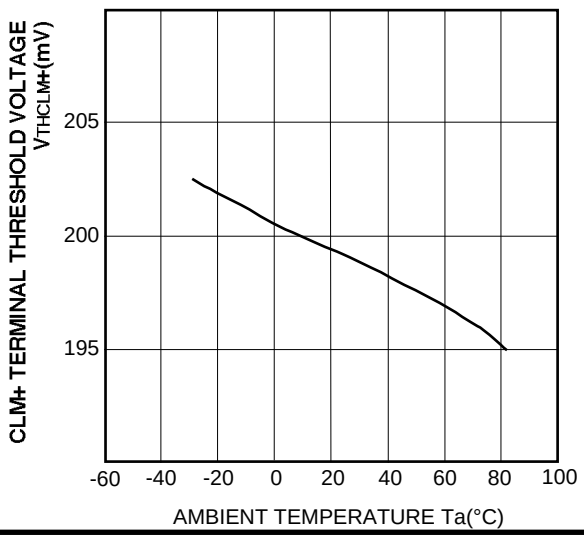
SOFT TERMINAL INPUT VOLTAGE VS.
EXPANSION RATE OF PERIOD



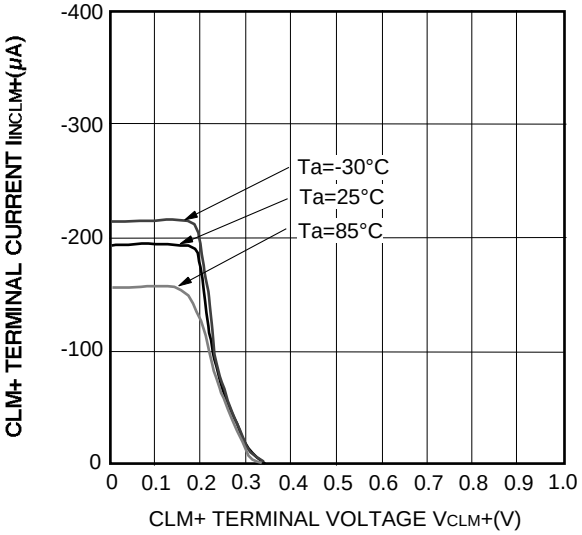
SOFT TERMINAL INPUT VOLTAGE VS.
INPUT VOLTAGE



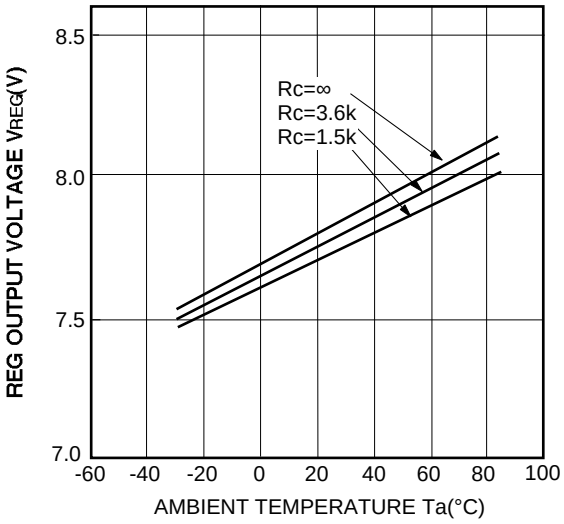
CLM+ TERMINAL THRESHOLD VOLTAGE
VS. AMBIENT TEMPERATURE



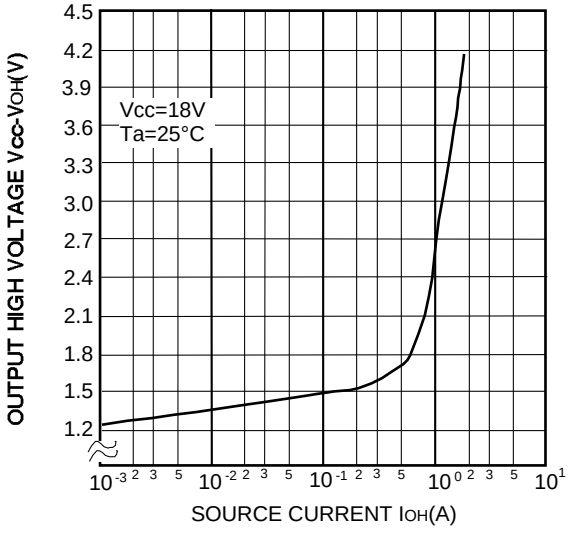
CLM+ TERMINAL CURRENT VS. CLM+ TERMINAL VOLTAGE



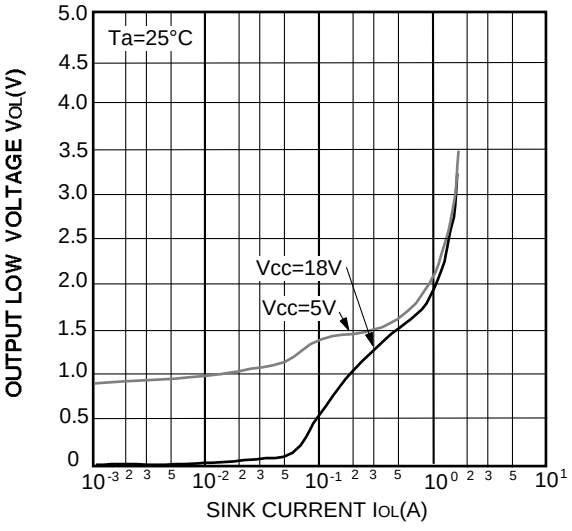
REG OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



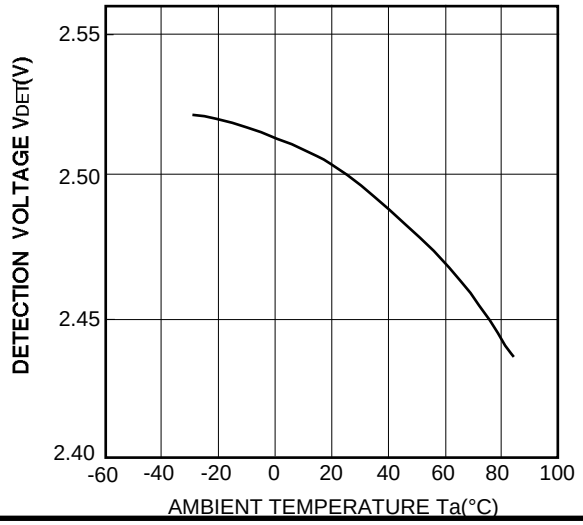
OUTPUT HIGH VOLTAGE VS. SOURCE CURRENT



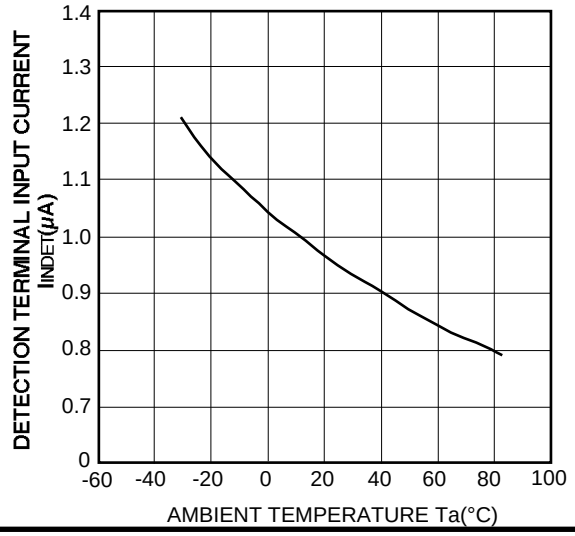
OUTPUT LOW VOLTAGE VS. SINK CURRENT



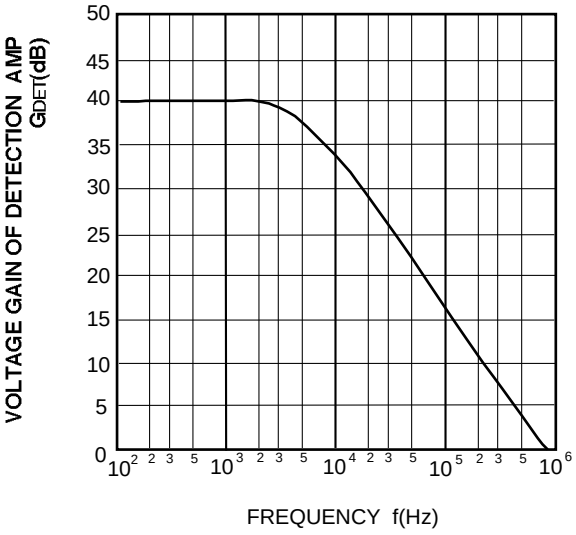
DETECTION VOLTAGE VS. AMBIENT TEMPERATURE



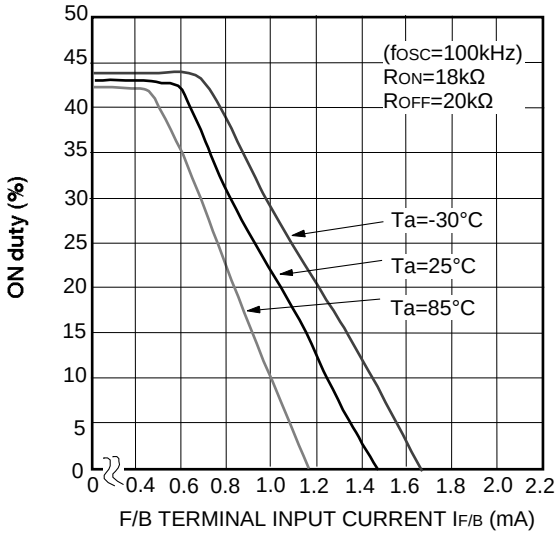
DETECTION TERMINAL INPUT CURRENT VS. AMBIENT TEMPERATURE



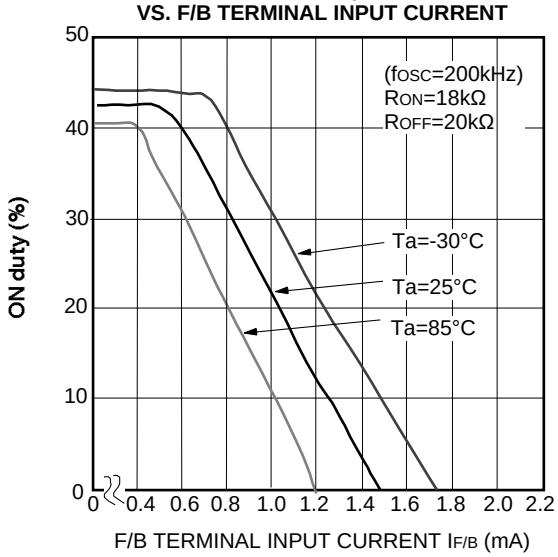
VOLTAGE GAIN OF DETECTION AMP VS. FREQUENCY



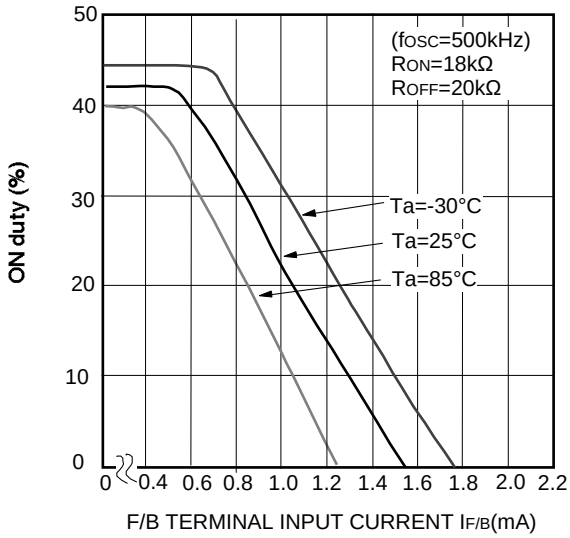
ON duty VS. F/B TERMINAL INPUT CURRENT



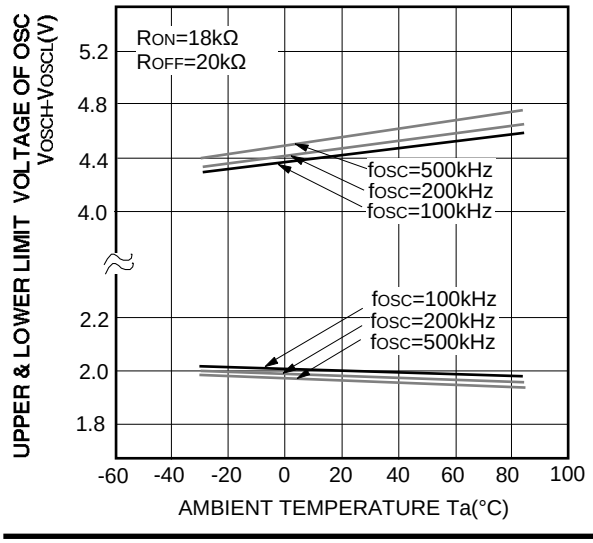
ON duty VS. F/B TERMINAL INPUT CURRENT



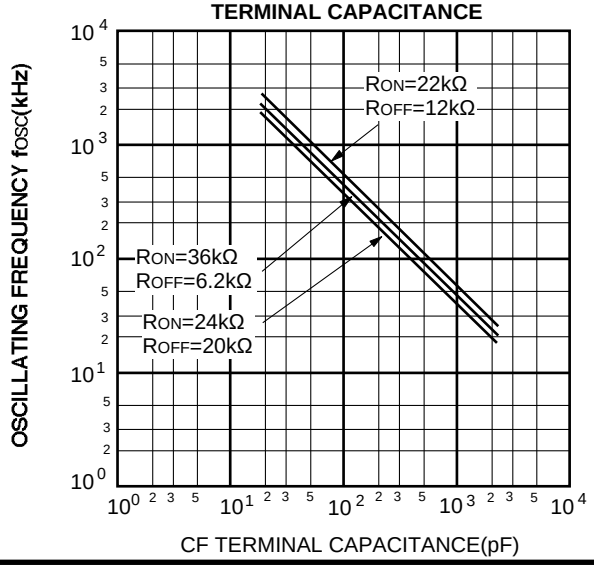
ON duty VS. F/B TERMINAL INPUT CURRENT



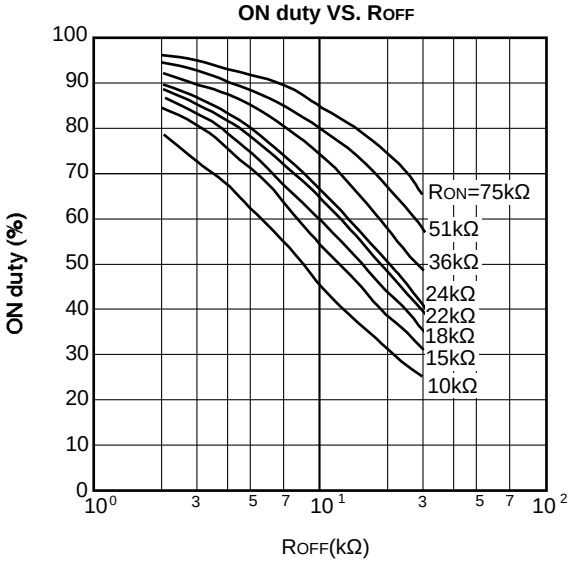
UPPER & LOWER LIMIT VOLTAGE OF OSC VS. AMBIENT TEMPERATURE



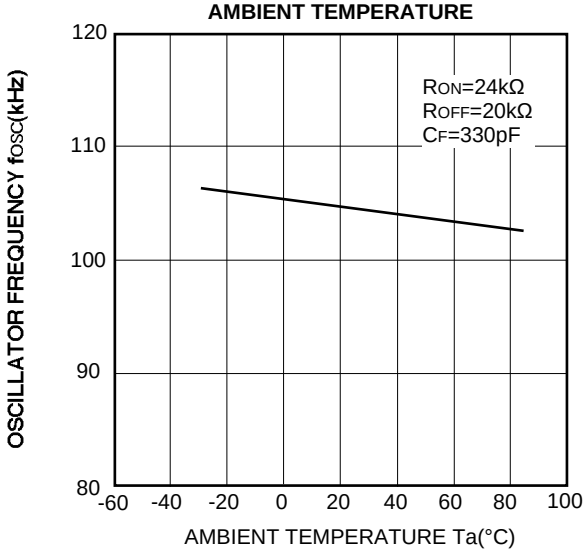
OSCILLATING FREQUENCY VS. CF TERMINAL CAPACITANCE



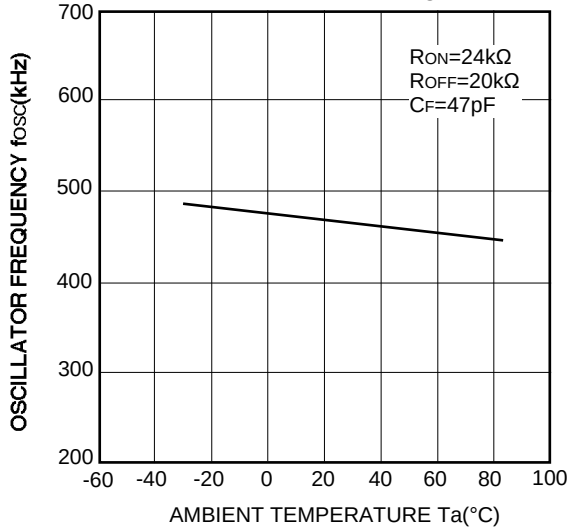
ON duty VS. ROFF



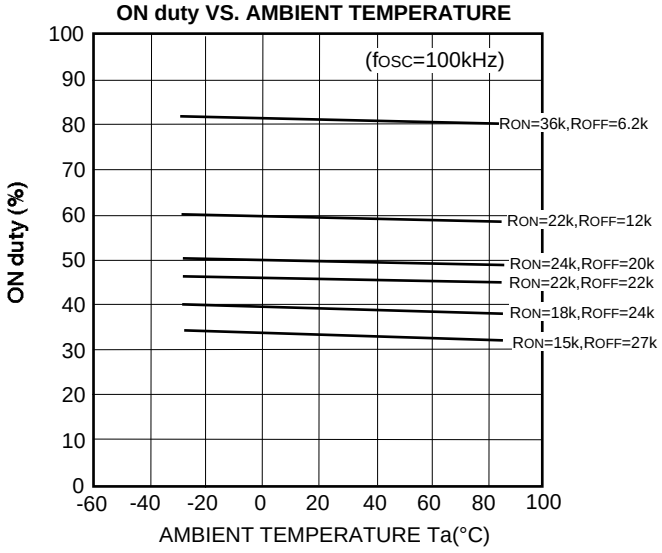
OSCILLATOR FREQUENCY VS. AMBIENT TEMPERATURE



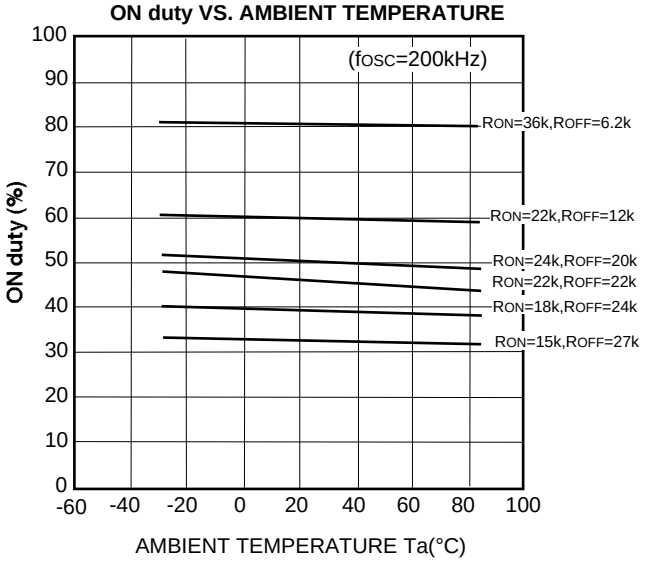
OSCILLATOR FREQUENCY VS. AMBIENT TEMPERATURE



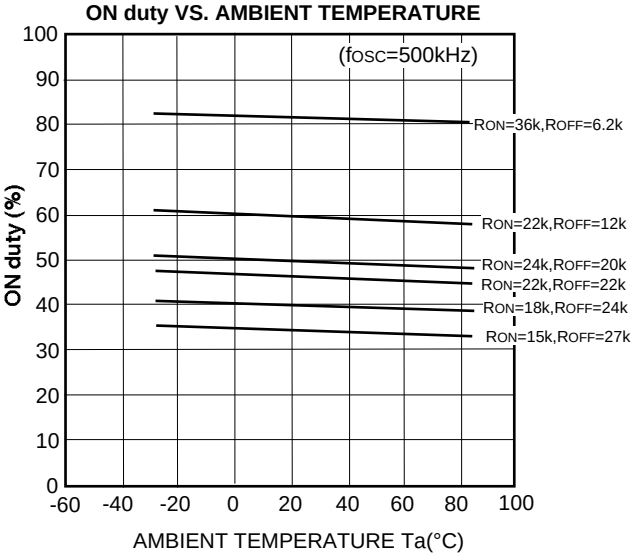
ON duty VS. AMBIENT TEMPERATURE



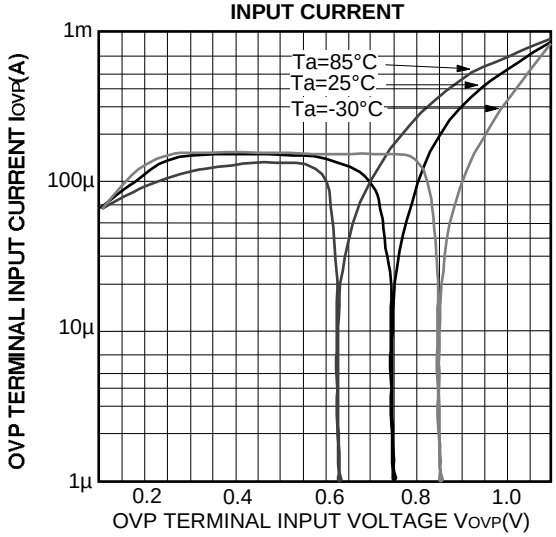
ON duty VS. AMBIENT TEMPERATURE



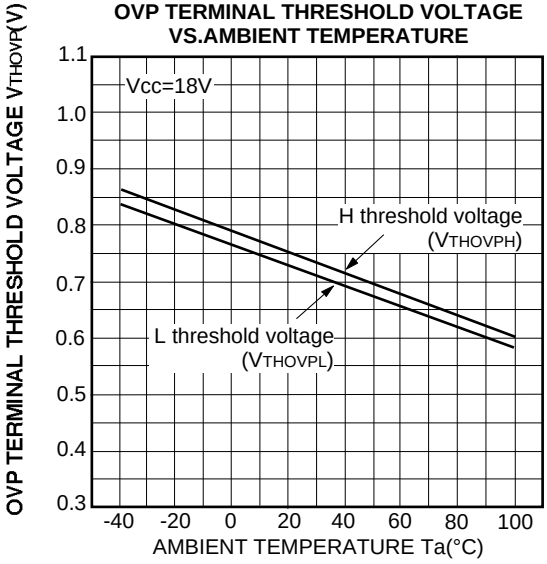
ON duty VS. AMBIENT TEMPERATURE



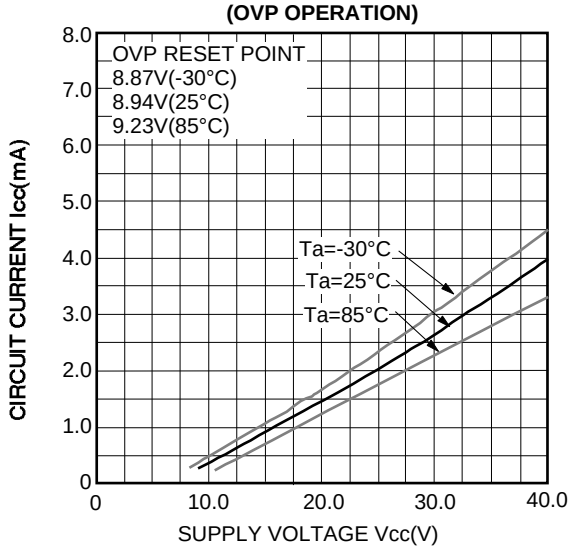
OVP TERMINAL INPUT VOLTAGE VS. INPUT CURRENT



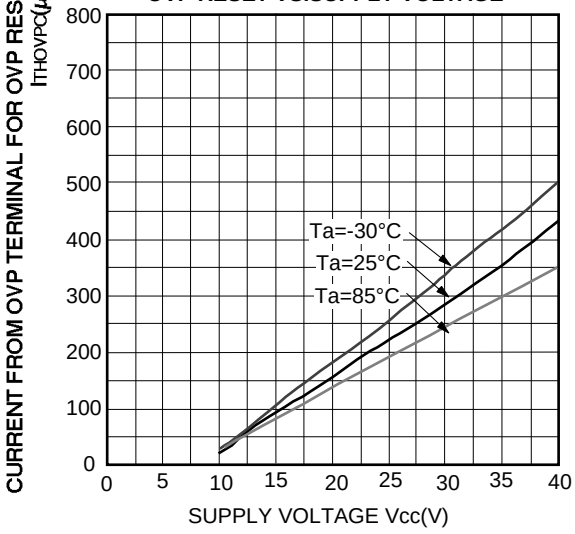
OVP TERMINAL THRESHOLD VOLTAGE VS.AMBIENT TEMPERATURE



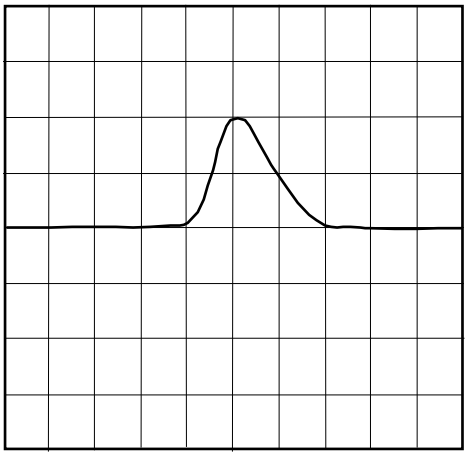
CIRCUIT CURRENT VS.SUPPLY VOLTAGE (OVP OPERATION)



CURRENT FROM OVP TERMINAL FOR OVP RESET VS.SUPPLY VOLTAGE

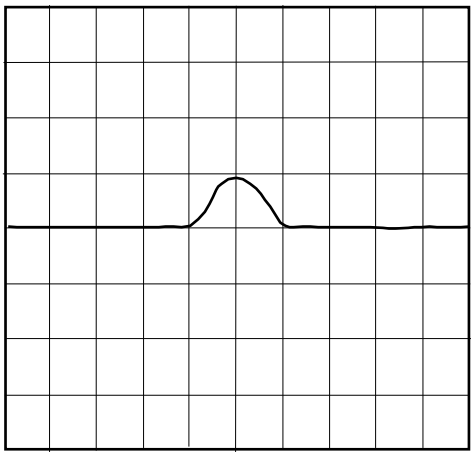


OUTPUT THRUGH CURRENT WAVEFORM AT RISING EDGE OF OUTPUT PULSE



Horizontal-axis : 20ns/div
Vertical-axis : 50mA/div

AT FALLING EDGE OF OUTPUT PULSE



Horizontal-axis : 20ns/div
Vertical-axis : 5mA/div

FUNCTION DESCRIPTION

Type M51996AP and M51996AFP are especially designed for off-line primary PWM control IC of switching mode power supply to get DC voltage from AC power supply.
Using this IC,smart SMPS can be realized with reasonable cost and compact size as the number of external electric parts can be reduced and also parts can be replaced by reasonable one.
In the following circuit diagram,MOS-FIT is used for output transistor,however bipolar transistor can be replaced with no problem.

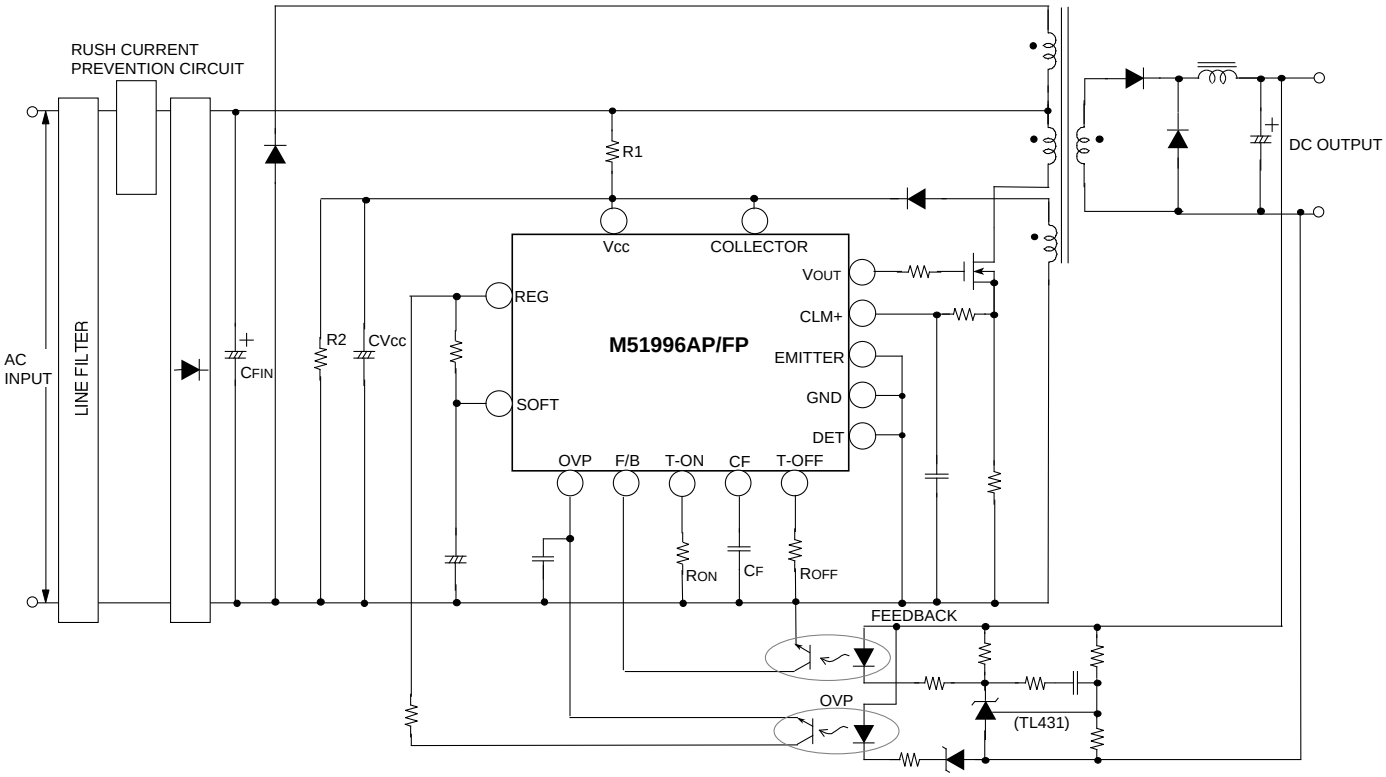


Fig.1 Application example for feed forward regulator

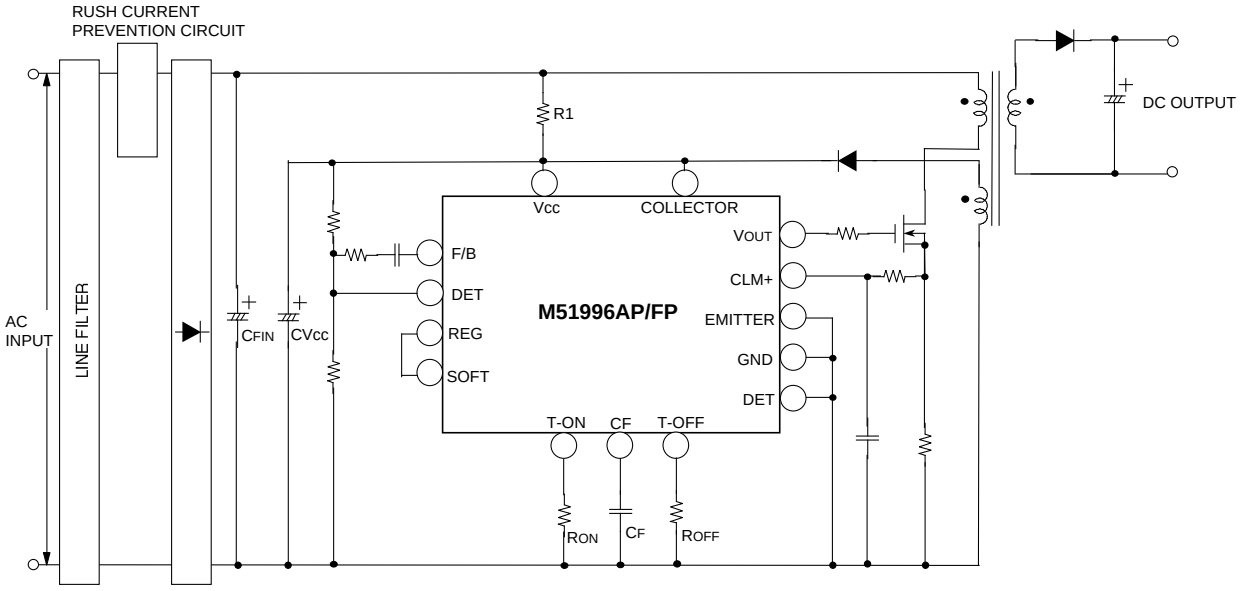


Fig.2 Application example for fly-back regulator

Start-up circuit section

The start-up current is such low current level as typical 100µA,as shown in Fig.3,when the Vcc voltage is increased from low level to start-up voltage Vcc(START).
In this voltage range,only a few parts in this IC,which has the function to make the output voltage low level,is alive and Icc current is used to keep output low level.The large voltage difference between Vcc(START) and Vcc(STOP) makes start-up easy,because it takes rather long duration from Vcc(START) to Vcc(STOP).

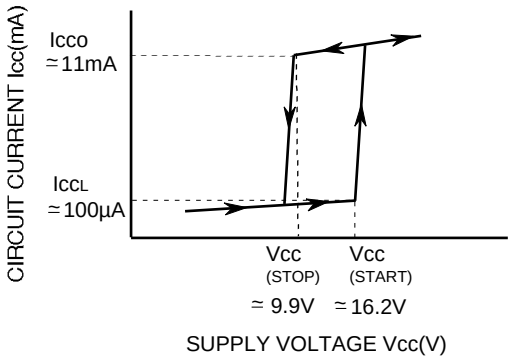


Fig.3 Circuit current vs.supply voltage

Oscillator section

The oscillation waveform is the triangle one.The ON-duration of output pulse depends on the rising duration of the triangle waveform and dead-time is decided by the falling duration.
The rising duration is determined by the product of external resistor RON and capacitor CF and the falling duration is mainly determined by the product of resistor ROFF and capacitor CF.

(1)Oscillator operation when SOFT circuit does not operate

Fig.4 shows the equivalent charging and discharging circuit diagram of oscillator.
The current flows through RON from the constant voltage source of 5.8V.CF is charged up by the same amplitude as RON current,when internal switch SW1,SW2 is switched to "charging side".The rise rate of CF terminal is given as

$$\simeq \frac{V_{T\text{ - ON}}}{R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(1)}$$

where $V_{T\text{ - ON}} \simeq$ 4.5V

The maximum on duration is approximately given as

$$\simeq \frac{(V_{OSCH}\text{-}V_{OSCL}) \times R_{ON} \times C_F}{V_{T\text{ - ON}}} \text{ (s)} \quad \text{.....(2)}$$

where $V_{OSCH} \simeq$ 4.4V
$V_{OSCL} \simeq$ 2.0V

CF is discharged by the summed-up of ROFF current and one sixteenth (1/16) of RON current by the function of Q2,Q3 and Q4 when SW1,SW2 are switched to "discharge side".

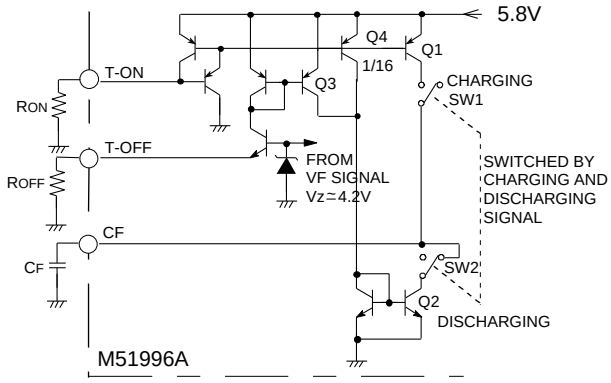


Fig.4 Schematic diagram of charging and discharging control circuit for OSC.capacitor CF

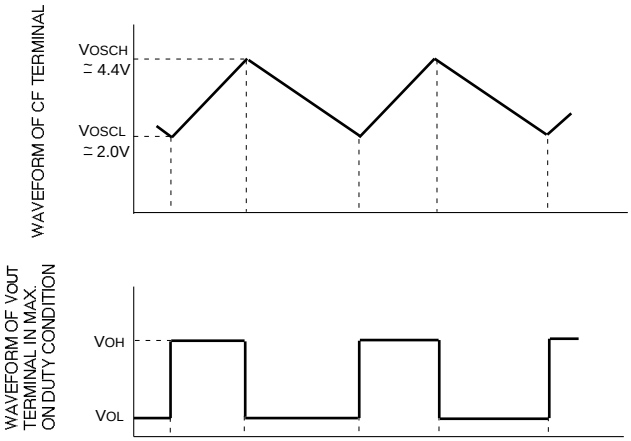


Fig.5 OSC.waveform at normal condition (no-operation of intermittent action and OSC.control circuit)

So fall rate of CF terminal is given as

$$\simeq \frac{V_{T\text{ - OFF}}}{R_{OFF} \times C_F} + \frac{V_{T\text{ - ON}}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \text{.....(3)}$$

The minimum off duration approximately is given as

$$\simeq \frac{(V_{OSCH}\text{-}V_{OSCL}) \times C_F}{\frac{V_{T\text{-OFF}}}{R_{OFF}} + \frac{V_{T\text{-ON}}}{16 \times R_{ON}}} \text{ (s)} \quad \text{.....(4)}$$

where $V_{T\text{ - OFF}} \simeq$ 3.5V

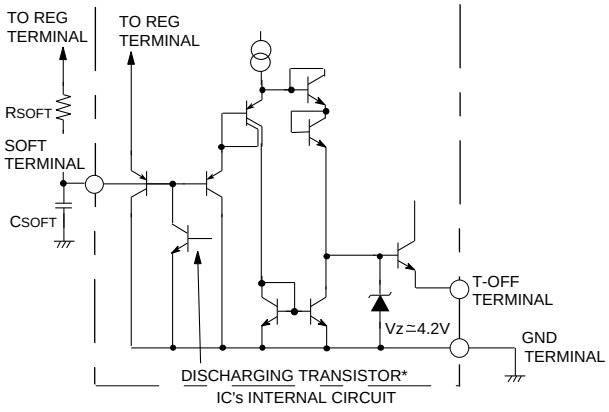
The cycle time of oscillation is given by the summation of Equations 2 and 4.
The frequency including the dead-time is not influenced by the temperature because of the built-in temperature compensating circuit.

(2)Oscillator operation when the SOFT(soft start) circuit is operating.

Output transistor is protected from rush current by CLM function at the start time of power on.SOFT terminal is used to improve the rising response of the output voltage of power supply(prevention of overshooting).
The ON duration of output is kept constant,and the OFF duration is extended as the SOFT terminal voltage becomes lower by the soft start circuit of this IC.
The maximum value of extension is set internally at approximately sixteen times of the maximum ON duartion.
The features of this method are as follows:

① It is ideal for primary control as IC driving current is supplied from the third widing of the main transformer at the start-up because constant ON duration is obtained from start-up.
② It is possible to get a wide dynamic range for ON/OFF ratio by pulse-by-pulse current limit circuit.
③ The response characteristics at power-on is not affected by input voltage as the pulse-by-pulse limit current value is not affected by the input voltage.

Fig.6 shows the circuit diagram of the soft start.If SOFT terminal voltage is low,T-OFF terminal voltage bocomes low and $V_{T\text{-}OFF}$ in equations (3) and (4) become low.



*Active when operation stops.

Fig.6 Circuit diagram of SOFT terminal section and T-OFF terminal section

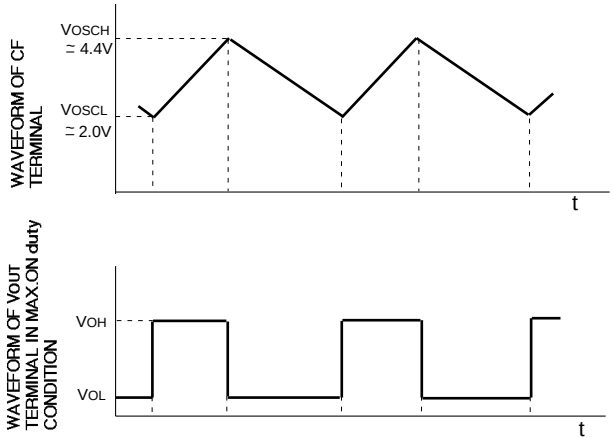


Fig.7 Oscillator waveform when the SOFT circuit is operating

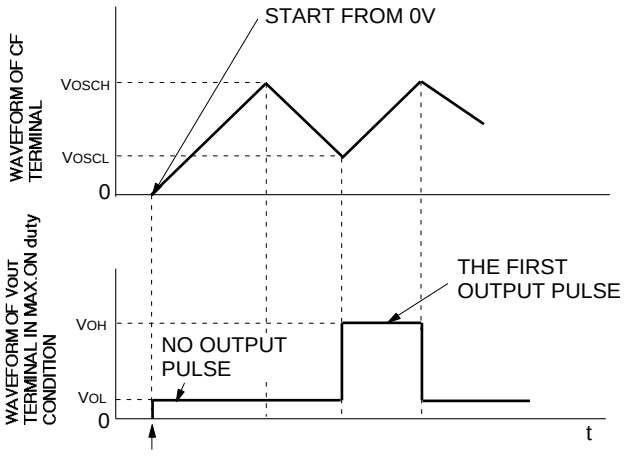


Fig.8 Relationship between oscillator waveform and output waveform at start-up

Fig.7 shows the relationship between oscillator waveform and output pulse.
If the SOFT terminal voltage is V_{SOFT},the rise rate of CF terminal given as

$$\simeq \frac{V_{T\text{ - ON}}}{R_{ON} \bullet C_F} \text{ (V/S)} \quad \text{.....(5)}$$

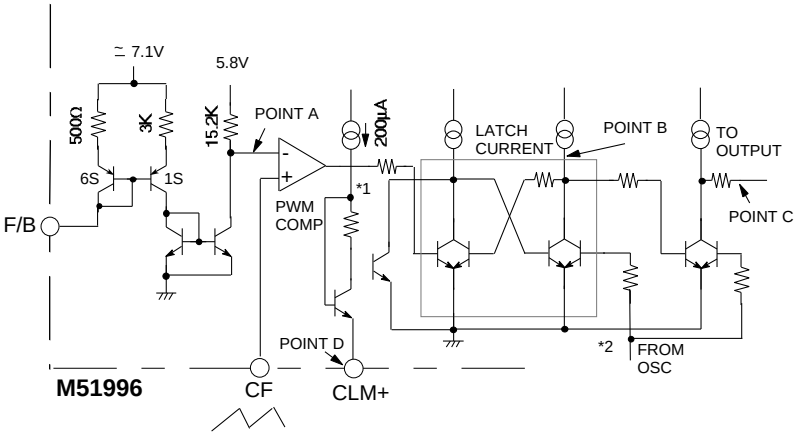
The fall rate of oscillation waveform is given as

$$\simeq \frac{V_{SOFT} - V_{BE}}{R_{ON} \bullet C_F} + \frac{V_{T\text{ - ON}}}{16 \bullet R_{ON} \bullet C_F} \text{ (V/S)} \quad \text{.....(6)}$$

where
V_{SOFT};SOFT terminal applied voltage
$V_{BE} \simeq 0.65V$
If $V_{SOFT} - V_{BE} < 0$, $V_{SOFT} - V_{BE} = 0$
If $V_{SOFT} - V_{BE} > V_{T\text{ - OFF}}$ (≃3.5V), $V_{SOFT} - V_{BE} = V_{T\text{ - OFF}}$

PWM comparator, PWM latch and current limit latch section

Fig.9 shows the scematic diagram of PWM comparator and PWM latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform,when the no output current flows from F/B terminal.
When the F/B terminal has finite impedance and current flows out from F/B terminal,"A" point potential shown in Fig.9 depends on this current.So the "A" point potential is close to GND level when the flow-out current becomes large.
"A" point potential is compared with the CF terminal oscillator waveform and PWM comparator,and the latch circuit is set when the potential of oscillator waveform is higher than "A" point potential.
The latch circuit is reset during the dead-time of oscillation (falling duration of oscillation current).So the "B" point potential or output waveform of latch circuit is the one shown in Fig.10.
The final output waveform or "C" point potential is got by combining the "B" point signal and dead-time signal logically.(please refer to Fig.10)



*1 Resistor to determine current limit sensitivity
*2 High level during dead time

Fig.9 PWM comparator PWM latch and current limit latch section

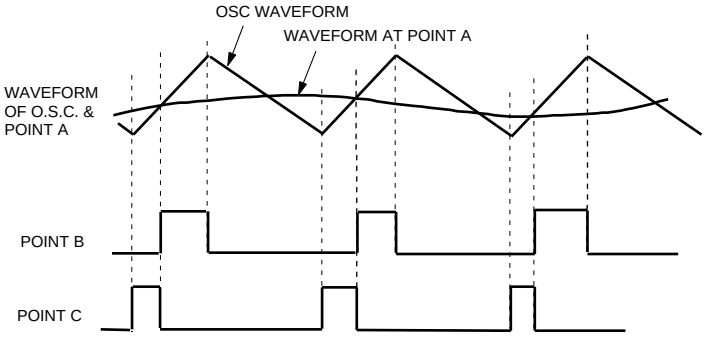


Fig.10 Waveforms of PWM comparator input point A, latch circuit points B and C

Current limiting section

When the current-limit signal is applied before the crossing instant of "A" pint potential and CF terminal voltage shown in Fig.9,this signal makes the output "off" and the off state will continue until next cycle.Fig.11 shows the timing relation among them.
If the current limiting circuit is set,no waveform is generated at output terminal, however this state is reset during the succeeding dead-time.
So this current limiting circuit is able to have the function in every cycle,and is named "pulse-by-pulse current limit".
There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.

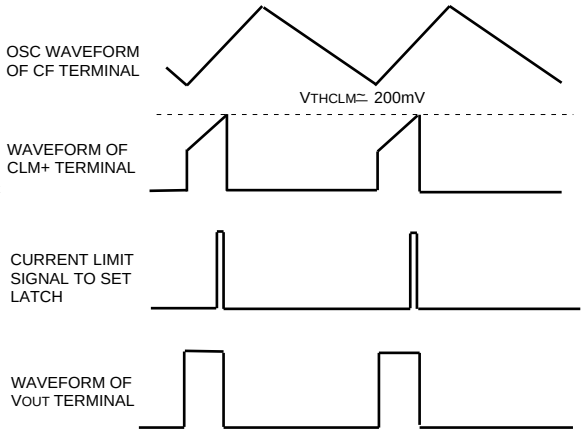


Fig.11 Operating waveform of current limiting circuit

To eliminate the abnormal operation by the noise voltage,the low pass filter,which consists of R_{NF} and C_{NF} is used as shown in Fig.12.
It is recommended to use 10 to 100Ω for R_{NF} because such range of R_{NF} is not influenced by the flow-out current of some 200μA from C_{LM+} terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

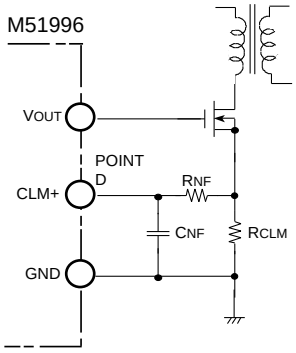


Fig.12 Connection diagram of current limit circuit

Voltage detector circuit(DET) section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.
The circuit diagram is quite similar to that of shunt regulator type 431 as shown in Fig.13.As well known from Fig.13 and Fig.14,the output of OP AMP has the current-sink ability,when the DET terminal voltage is higher than 2.5V

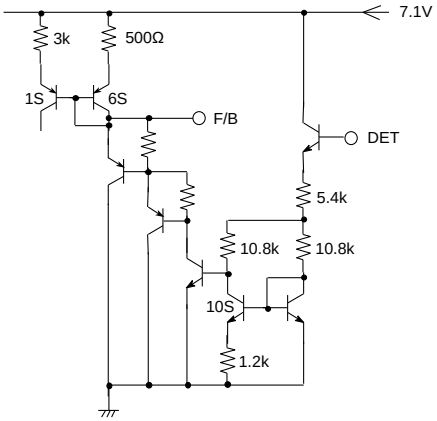


Fig.13 Voltage detector circuit section(DET)

but it becomes high impedance state when lower than 2.5V DET terminal and F/B terminal have inverting phase characteristics each other,so it is recommended to connect the resistor and capacitor in series between them for phase compensation.It is very important one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

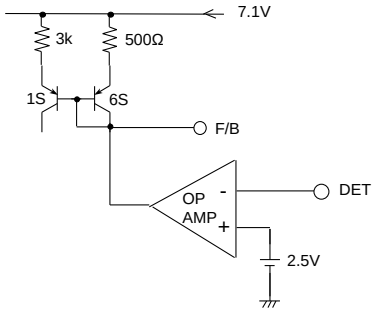


Fig.14 Schmatic diagram of voltage detector circuit section(DET)

OVP circuit(over voltage protection circuit)section

OVP circuit is basically positive feedback circuit constructed by Q2,Q3 as shown in Fig.15.
Q2,Q3 turn on and the circuit operation of IC stops,when the input signal is applied to OVP terminal.(threshold voltage ≃ 750mV)
The current value of I2 is about 150μA when the OVP does not operates but it decreases to about 2μA when OVP operates.

It is necessary to input the sufficient larger current(800μA to 8mA)than I2 for triggering the OVP operation.
The reason to decrease I2 is that it is necessary that Icc at the OVP rest supply voltage is small.
It is necessary that OVP state holds by circuit current from R1 in the application example,so this IC has the characteristic of small Icc at the OVP reset supply voltage(≃stand-by current + 20μA)
On the other hand,the circuit current is large in the higher supply voltage,so the supply voltage of this IC doesn't become so high by the voltage drop across R1.
This characteristic is shown in Fig.16.
The OVP terminal input current in the voltage lower than the OVP threshold voltage is based on I2 and the input current in the voltage higher than the OVP threshold voltage is the sum of the current flowing to the base of Q3 and the current flowing from the collector of Q2 to the base.
For holding in the latch state,it is necessary that the OVP terminal voltage is kept in the voltage higher than V_{BE} of Q3.
So if the capacitor is connected between the OVP terminal and GND,even though Q2 turns on in a moment by the surge voltage,etc,this latch action does not hold if the OVP terminal voltage does not become higher than V_{BE} of Q3 by charging this capacitor.
For resetting OVP state,it is necessary to make the OVP terminal voltage lower than the OVP L threshold voltage or make Vcc lower than the OVP reset supply voltage.
As the OVP reset voltage is settled on the rather high voltage of 9.0V,SMPS can be reset in rather short time from the switch-off of the AC power source if the smoothing capacitor is not so large value.

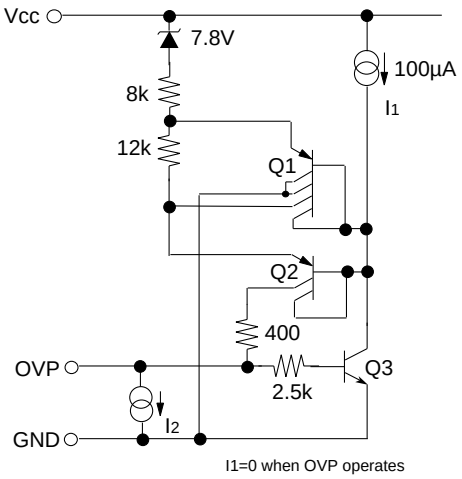


Fig.15 Detail diagram of OVP circuit

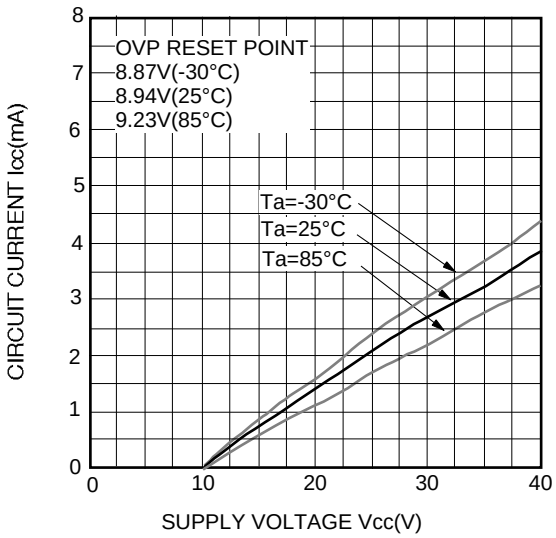


Fig.16 CIRCUIT CURRENT VS. SUPPLY VOLTAGE (OVP OPERATION)

Output section

It is required that the output circuit have the high sink and source abilities for MOS-FET drive.It is well known that the "totempole circuit has high sink and source ability.However,it has the demerit of high through current.
For example,the through current may reach such the high current level of 1A,if type M51996A has the "conventional" totempole circuit.For the high frequency application such as higher than 100kHz,this through current is very important factor and will cause not only the large Icc current and the inevitable heat-up of IC but also the noise voltage.
This IC uses the improved totempole circuit,so without deteriorating the characteristic of operating speed,its through current is approximately 100mA.

APPLICATION NOTE OF TYPE M51996AP/FP

Design of start-up circuit and the power supply of IC

(1)The start-up circuit when it is not necessary to set the start and stop input voltage

Fig.17 shows one of the example circuit diagram of the start-up circuit which is used when it is not necessary to set the start and stop voltage.
It is recommended that the current more than 300μA flows through R1 in order to overcome the operation start-up current Icc(START) and Cvcc is in the range of 10 to 47μF.The product of R1 by Cvcc causes the time delay of operation,so the response time will be long if the product is too much large.

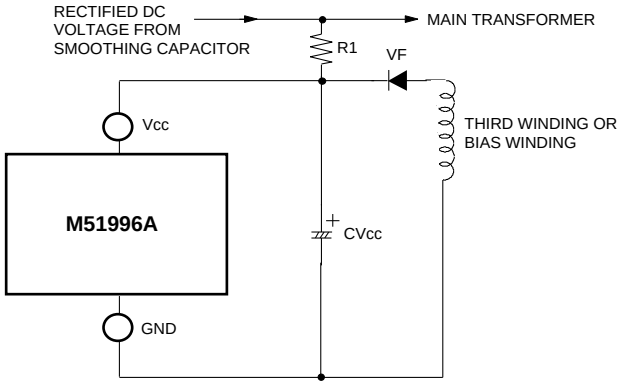


Fig.24 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

Just after the start-up,the Icc current is supplied from Cvcc,however,under the steady state condition ,IC will be supplied from the third winding or bias winding of transformer,the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage Vcc(STOP).
The Vcc voltage is recommended to be 12V to 17V as the normal and optimum gate voltage is 10 to 15V and the output voltage(VOH) of type M51996AP/FP is about(Vcc-2V).
It is not necessary that the induced voltage is settled higher than the operation start-up voltage Vcc(START),and the high gate drive voltage causes high gate dissipation,on the other hand,too low gate drive voltage does not make the MOS-FET fully on-state or the saturation state.

(2)The start-up circuit when it is not necessary to set the start and stop input voltage

It is recommend to use the third winding of "forward winding" or "positive polarity" as shown in Fig.18,when the DC source voltages at both the IC operation start and stop must be settled at the specified values.
The input voltage(VIN(START)),at which the IC operation starts,is decided by R1 and R2 utilizing the low start-up

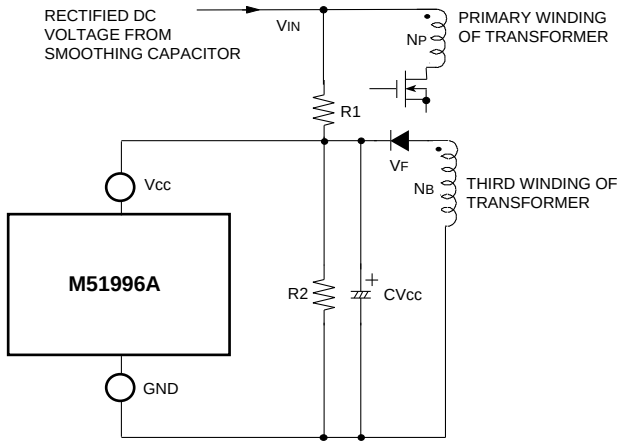


Fig.18 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

current characteristics of type M51996AP/FP.
The input voltage($V_{IN(STOP)}$),at which the IC operation stops,is decided by the ratio of third winding of transformer.
The $V_{IN(START)}$ and $V_{IN(STOP)}$ are given by following equations.

$$V_{IN(START)} \simeq R1 \cdot I_{CCL} + \left(\frac{R1}{R2} + 1\right) \cdot V_{CC(START)} \quad \text{.....(7)}$$

$$V_{IN(STOP)} \simeq (V_{CC(STOP)} - V_F) \cdot \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP(P-P)} \quad \text{.....(8)}$$

where

I_{CCL} is the operation start-up current of IC
$V_{CC(START)}$ is the operation start-up voltage of IC
$V_{CC(STOP)}$ is the operation stop voltage of IC
V_F is the forward voltage of rectifier diode
$V'_{IN(P-P)}$ is the peak to peak ripple voltage of

Vcc terminal $\simeq \frac{N_B}{N_P} V'_{IN\ RIP(P-P)}$

It is required that the $V_{IN(START)}$ must be higher than $V_{IN(STOP)}$. When the third winding is the "fly back winding" or "reverse polarity",the $V_{IN(START)}$ can be fixed,however,$V_{IN(STOP)}$ can not be settled by this system,so the auxiliary circuit is required.

(3)Notice to the Vcc,Vcc line and GND line

To avoid the abnormal IC operation,it is recommended to design the Vcc is not vary abruptly and has few spike voltage,which is induced from the stray capacity between the winding of main transformer.
To reduce the spike voltage,the Cvcc,which is connected between Vcc and ground,must have the good high frequency characteristics.
To design the conductor-pattern on PC board,following cautions must be considered as shown in Fig.19.
(a)To separate the emitter line of type M51996A from the GND line of the IC
(b)The locate the C_{VCC} as near as possible to type M51996A and connect directly
(c)To separate the collector line of type M51996A from the Vcc line of the IC
(d)To connect the ground terminals of peripheral parts of ICs to GND of type M51996A as short as possible

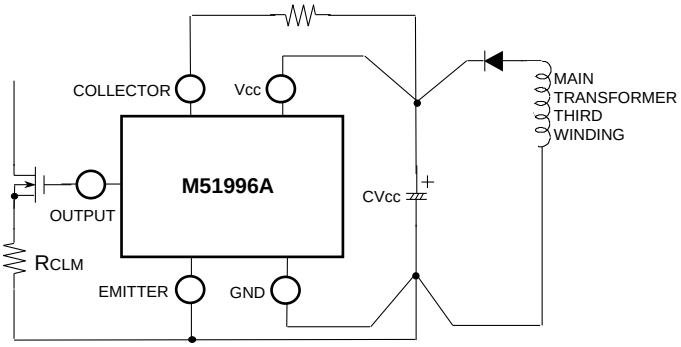


Fig.19 How to design the conductor-pattern of type M51996A on PC board(schematic example)

(4)Power supply circuit for easy start-up

When IC start to operate,the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the Icc of the IC increases abruptly.In case shown in Fig.17 and 18,some "unstable start-up" or "fall to start-up" may happen, as the charging interval of C_{VCC} is very short duration;that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage,if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51996A.
It is recommended to use the 10 to 47μF for C_{VCC1},and about 5 times capacity bigger than C_{VCC1} for C_{VCC2}.

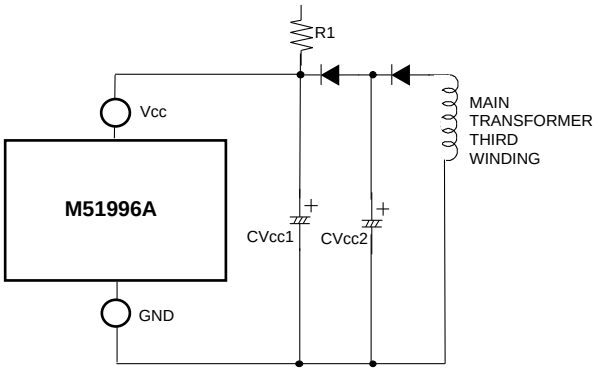


Fig.20 DC source circuit for stable start-up

OVP circuit

(1)To avoid the miss operation of OVP

It is recommended to connect the capacitor between OVP terminal and GND for avoiding the miss operation by the spike noise.
The OVP terminal is connected with the sink current source (≃150μA) in IC when OVP does not operate,for absorbing the leak current of the photo coupler in the application.
So the resistance between the OVP terminal and GND for leak-cut is not necessary.
If the resistance is connected,the supply current at the OVP reset supply voltage becomes large.
As the result,the OVP reset supply voltage may become higher than the operation stop voltage.
In that case,the OVP action is reset when the OVP is triggered at the supply voltage a little high than the operation stop voltage.
So it should be avoided absolutely to connect the resistance between the OVP terminal and GND.

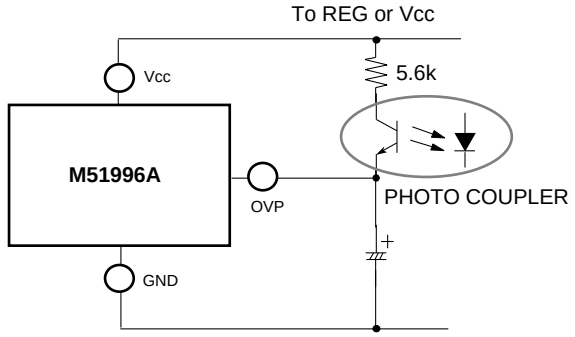


Fig.21 Peripheral circuit of OVP terminal

(2)Application circuit to make the OVP-reset time fast

The reset time may becomes problem when the discharge time constant of C_{FIN} • (R1+R2) is long. Under such the circuit condition,it is recommended to discharge the C_{VCC} forcedly and to make the Vcc low value;This makes the OVP-reset time fast.

(3)OVP setting method using the induced third winding voltage on fly back system

For the over voltage protection (OVP),the induced fly back type third winding voltage can be utilized,as the induced third winding voltage depends on the output voltage.Fig.23 shows one of the example circuit diagram.

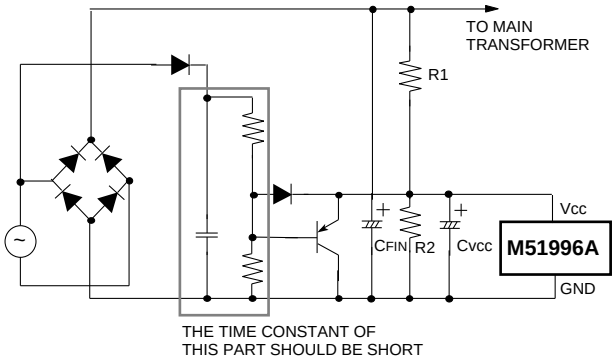


Fig.22 Example circuit diagram to make the OVP-reset-time fast

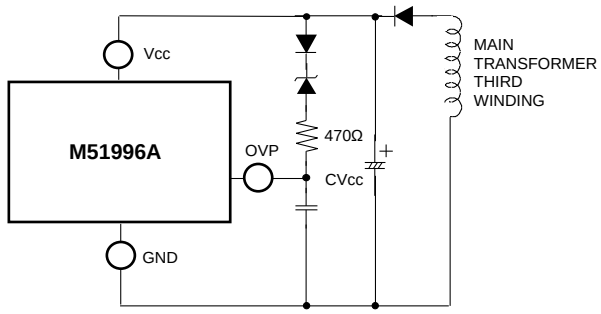


FIG.23 OVP setting method using the induced third winding voltage on fly back system

(4)Method to control for ON/OFF using the OVP terminal

You can reset OVP to lower the OVP terminal voltage lower than V_{THOVPL}.
So you can control for ON/OFF using this nature.
The application is shown in Fig.24.
The circuit turns off by SW OFF and turns on by SW ON in this application.
Of course you can make use of the transistor or photo-transistor instead of SW.

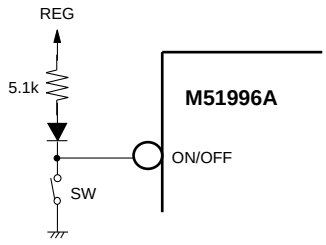


FIG.24 Method to control for ON/OFF using the OVP terminal

Current limiting circuit

(1)Peripheral circuit of CLM+ terminal

Fig.25 shows the example circuit diagrams around the CLM+ terminal.It is required to connect the low pass filter,in order to reduce the spike current component,as the main current or drain current contains the spike current especially during the turn-on duration of MOS-FIT.
1,000pF to 22,000pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the functions both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

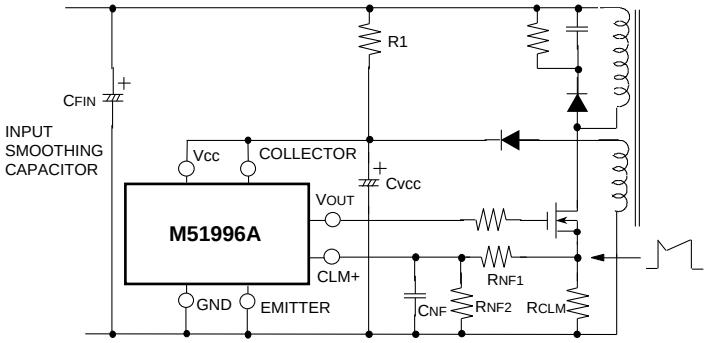


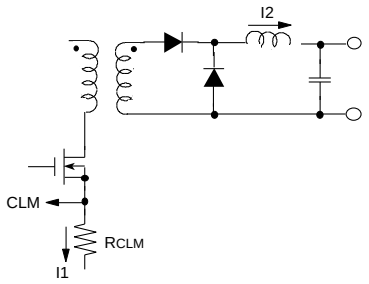
Fig.25 Peripheral circuit diagram of CLM+ terminal

To design the R_{NF1} and R_{NF2},it is required to consider the influence of CLM+ terminal source current(I_{INCLM+}), which value is in the range of 90 to 270μA.
In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2},(R_{NF1}/R_{NF2})is recommended to be less than 100Ω.
The R_{CLM} should be the non-inductive resistor.

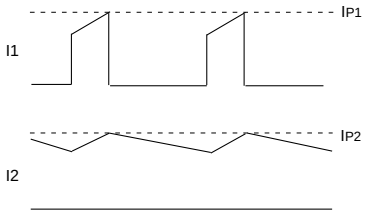
(2)Over current limiting curve

(a)In case of feed forward system

Fig.26 shows the primary and secondary current wave-forms under the current limiting operation.
At the typical application of pulse by pulse primary current detecting circuit,the secondary current depends on the primary current.As the peak value of secondary current is limited to specified value,the characteristics curve of output voltage versus output current become to the one as shown in Fig.27.



(a) Feed forward system



(b) Primary and secondary current

Fig.26 Primary and secondary current waveforms under the current limiting operation condition on feed forward system

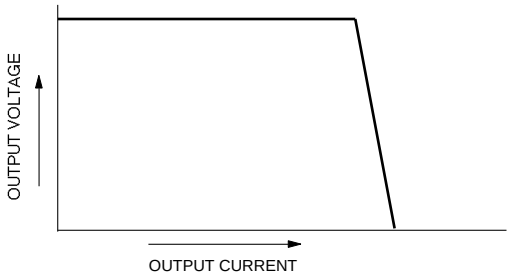


Fig.27 Over current limiting curve on feed forward system

The demerit of the pulse by pulse current limiting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM+ terminal and propagation delay time T_{PDCLM} from CLM+ terminal to output terminal of type M51996A.The typical T_{PDCLM+} is 100ns.
As the frequency becomes higher,the delay time must be shorter.And as the secondary output voltage becomes higher,the dynamic range of on-duty must be wider;it means that it is required to make the on-duration much more narrower. So this system has the demerit at the higher oscillating frequency and higher output voltage applications.
To prevent that the SOFT terminal is used to lower the frequency when the curve starts to become vertical.

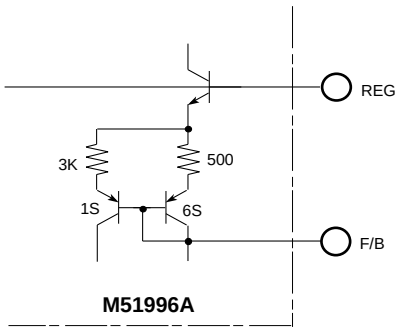


Fig.28 Relationship between REG terminal and F/B terminal

If the curve becomes vertical because of an excess current, the output voltage is lowered and no feedback current flows from feedback photo-coupler;the PWM comparator operates to enlarge the duty sufficiently,but the signal from the CLM+ section operates to make the pulse width narrower.
Under the condition in which I2 in Fig.26 does not become 0,the output voltage is proportional to the product of the input voltage VIN(primary side voltage of the main transformer) and on duty.If the bias winding is positive,Vcc is approximately proportional to VIN.The existance of feed back current of the photo-coupler is known by measuring the F/B terminal voltage which becomes less than 2VBE in the internal circuit of REG terminal and F/B terminal if the output current flows from the F/B terminal.
Fig.29 shows an application example.
Q1 is turned on when normal output voltage is controlled at a certain value.The SOFT terminal is clampedto a high-level voltage.If the output voltage decreases and the curve starts to drop,no feed back current flows,Q1 is turned off and the SOFT terminal responds to the smoothed output voltage.
It is recommended to use an R1 and R2 of 10kΩ~30kΩ.An R3 of 20 to 100kΩ and C of 1000pF to 8200pF should be used.
To change the knee point of frequency drop,use the circuit in Fig.30.
To have a normal SOFT start function in the circuit in Fig.29,use the circuit in Fig.31.It is recommended to use an R4 of 10kΩ.

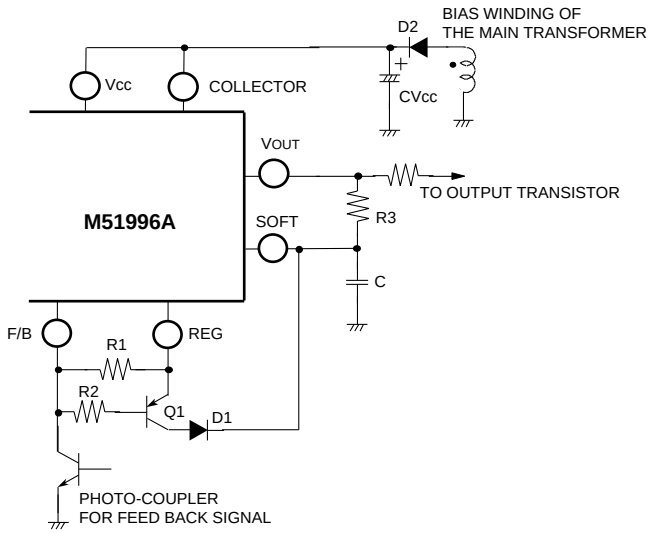


Fig.29 Current to lower frequency during over current

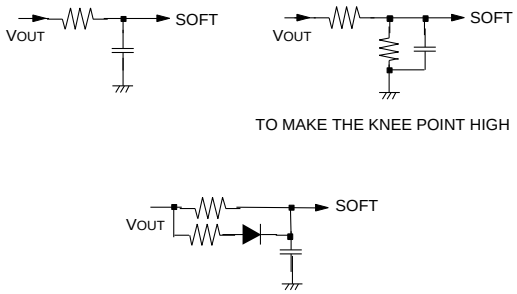


Fig.30 Method to control the knee point of frequency drop

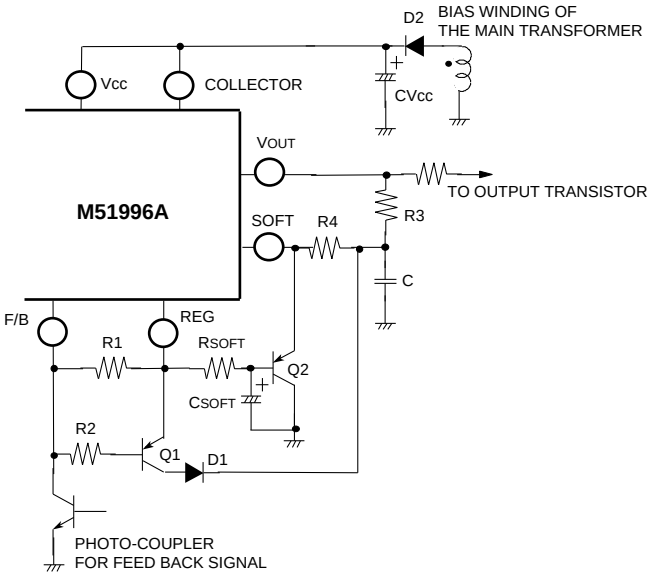


Fig.31 Circuit to use frequency drop during the over current and normal soft start

(b)In case of fly back system

The DC output voltage of SMPS depends on the Vcc voltage of type M51996A when the polarity of the third winding is negative and the system is fly back.So the operation of type M51996A will stop when the Vcc becomes lower than "Operation-stop voltage" of M51996A when the DC output voltage of SMPS decreases under specified value at over load condition. However,the M51996A will non-operate and operate intermittently,as the Vcc voltage rises in accordance with the decrease of Icc current.
The fly back system has the constant output power characteristics as shown in Fig.32 when the peak primary current and the operating frequency are constant.
Toavoid anincrease of the output current,the frequency is lowered when the DC output voltage of SMPS starts to drop using the SOFT terminal.Vcc is divided and is input to the SOFT terminal as shown in Fig.33,because the voltage in proportional to the output voltage is obtained from the bias winding.In this application example,the current flowing to R3 added to the start-up current.So please use high resistance or 100kΩ to 200kΩ for R3.
The start-up current is not affected by R3 if R3 is connected to Cvcc2 in the circuit shown in Fig.20.

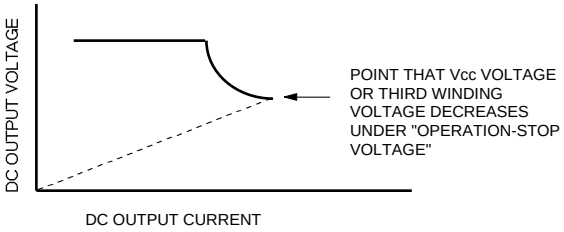


Fig.32 Over current limitting curve on fly back system

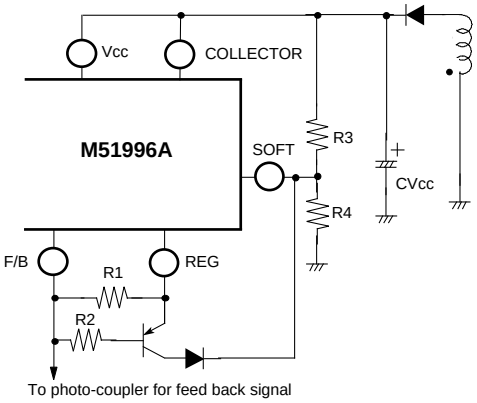


Fig.33 Current to lower the frequency during the over current in the fly back system

Output circuit

(1)The output terminal characteristics at the Vcc voltage lower than the "Operation-stop" voltage

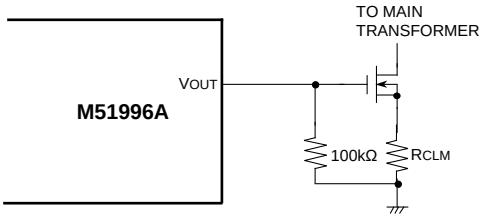


Fig.34 Circuit diagram to prevent the MOS-FIT gate potential rising

The output terminal has the current sink ability even though the Vcc voltage lower than the "Operation-stop" voltage or Vcc($_{STOP}$) (It means that the terminal is "Output low state" and please refer characteristics of output low voltage versus sink current.)
This characteristics has the merit not to damage the MOS-FIT at the stop of operation when the Vcc voltage decreases lower than the voltage of Vcc($_{STOP}$),as the gate charge of MOS-FIT,which shows the capacitive load characteristics to the output terminal,is drawn out rapidly.
The output terminal has the draw-out ability above the Vcc voltage of 2V,however,lower than the 2V,it loses the ability and the output terminal potential may rise due to the leakage current.
In this case, it is recommended to connect the resistor of 100kΩ between gate and source of MOS-FIT as shown in Fig.34.

(2)MOS-FIT gate drive power dissipation

Fig.35 shows the relation between the applied gate voltage and the stored gate charge.
In the region ① ,the charge is mainly stored at C_{GS} as the depletion is spread and C_{GD} is small owing to the off-state of MOS-FIT and the high drain voltage.
In the region ② ,the C_{GD} is multiplied by the "mirror effect" as the characteristics of MOS-FIT transfers from off-state to on-state.
In the region ③ ,both the C_{GD} and C_{GS} affect to the characteristics as the MOS-FIT is on-state and the drain voltage is low.
The charging and discharging current caused by this gate charge makes the gate power dissipation.The relation between gate drive current I_D and total gate charge Q_{GSH} is shown by following equation;

$$I_D = Q_{GSH} \cdot f_{OSC} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (11)$$

Where

f_{OSC} is switching frequency

As the gate drive current may reach up to several tenths milliamperes at 500kHz operation,depending on the size of MOS-FIT,the power dissipation caused by the gate current can not be neglected.
In this case,following action will be considered to avoid heat up of type M51996A.

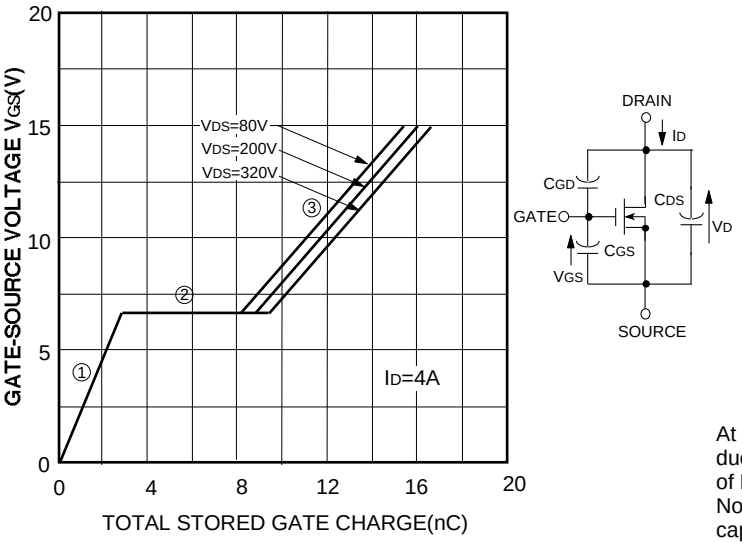


Fig.35 The relation between applied gate-source voltage and stored gate charge

(1) To attach the heat sink to type M51996A
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

(3)Output buffer circuit

It is recommended to use the output buffer circuit as shown in Fig.36,when type M51996A drives the large capacitive load or bipolar transistor.

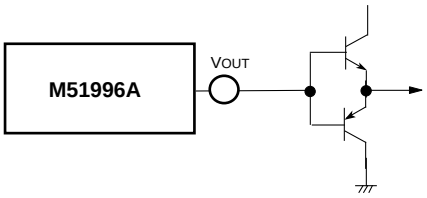


Fig.36 Output buffer circuit diagram

DET

Fig.37 shows how to use the DET circuit for the voltage detector and error amplifier.
For the phase shift compensation,it is recommended to connected the CR network between det terminal and F/B terminal.

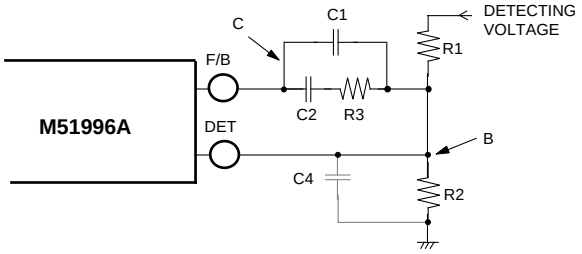


Fig.37 How to use the DET circuit for the voltage detector

Fig.38 shows the gain-frequency characteristics between point B and point C shown in Fig.37.
The G1,ω_1 and ω_2 are given by following equations;

$$G1 = \frac{R3}{R1/R2} \quad \text{.....(10)}$$

$$\omega_1 = \frac{1}{C2 \cdot R3} \quad \text{.....(11)}$$

$$\omega_2 = \frac{C1 + C2}{C1 \cdot C2 \cdot R3} \quad \text{.....(12)}$$

At the start of the operation,there happen to be no output pulse due to F/B terminal current through C1 and C2,as the potential of F/B terminal rises sharply just after the start of the operation. Not to lack the output pulse,is recommended to connect the capacitor C4 as shown by broken line.
Please take notice that the current flows through the R1 and R2 are superposed to ICC(START).Not to superpose,R1 is connected to Cvcc2 as shown in Fig.20.

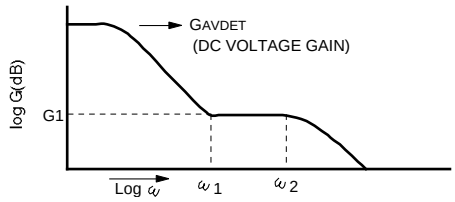


Fig.38 Gain-frequency characteristics between point B and C shown in Fig.37

How to get the narrow pulse width during the start of operation

Fig.39 shows how to get the narrow pulse width during the start of the operation.If the pulse train of forcedly narrowed pulse-width continues too long,the misstart of operation may happen,so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation.0.1µF is recommended for the C.

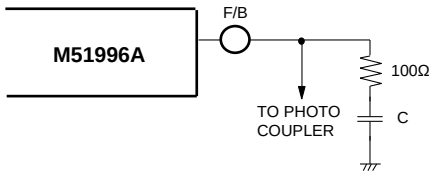


Fig.39 How to get the narrow pulse width during the start of operation

Driver circuit for bipolar transistor

When the bipolar transistor is used instead of MOS-FIT,the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration,in order to make the switching speed of bipolar transistor fast one. In this case,over current can not be detected by detecting resistor in series to bipolar transistor,so it is recommended to use the CT(current transformer).
For the low current rating transistor,type M51996A can drive it directly as shown in Fig.42.

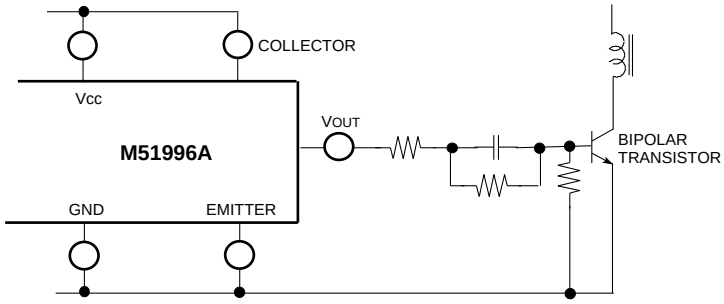


Fig.42 Driver circuit diagram (2) for bipolar transistor

How to synchronize with external circuit

Type M51996A has no function to synchronize with external circuit,however,there is some application circuit for synchronization as shown in Fig.40.

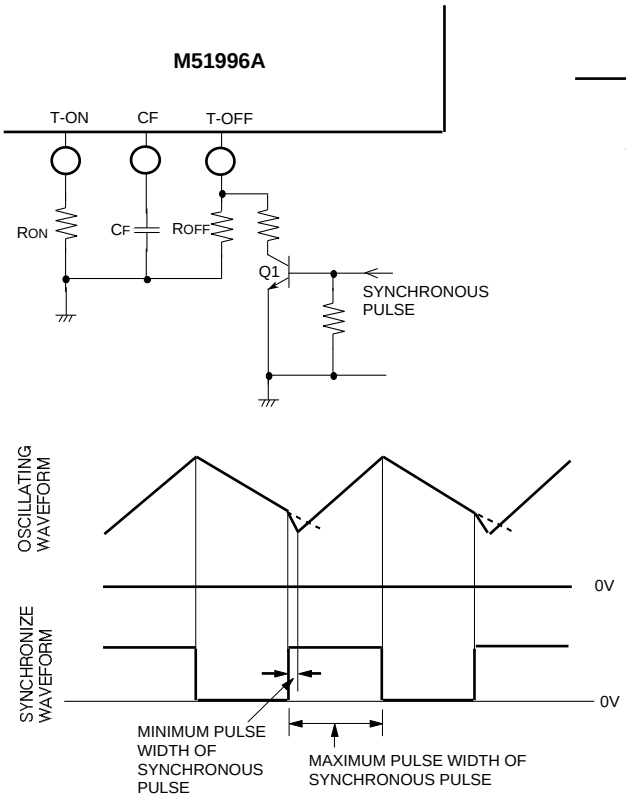


Fig.40 How to synchronize with external circuit

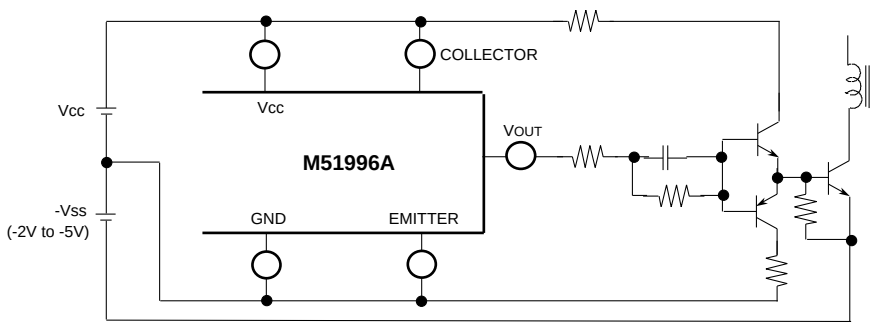


Fig.41 Driver circuit diagram (1) for bipolar transistor

Attention for heat generation

The maximum ambient temperature of type M51996A is +85°C,however,the ambient temperature in vicinity of the IC is not uniform and varies place by place,as the amount of power dissipation is fearfully large and the power dissipation is generated locally in the switching regulator.
So it is one of the good idea to check the IC package temperature.
The temperature difference between IC junction and the surface of IC package is 15°C or less,when the IC junction temperature is measured by temperature dependency of forward voltage of pin junction,and IC package temperature is measured by "thermo-viewer",and also the IC is mounted on the "phenol-base" PC board in normal atmosphere.
So it is concluded that the maximum case temperature(surface temperature of IC) rating is 120°C with adequate margin.