

# MC74HC4851A, MC74HC4852A

## Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

### Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/ resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

#### Features

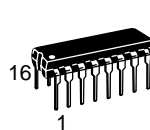
- Injection Current Cross-Coupling Less than 1mV/mA (See Figure 9)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- Pb-Free Packages are Available\*



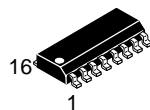
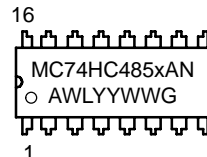
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<http://onsemi.com>

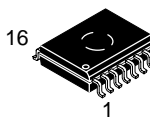
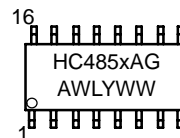
#### MARKING DIAGRAMS



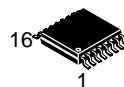
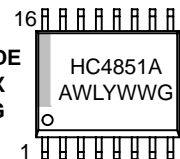
PDIP-16  
N SUFFIX  
CASE 648



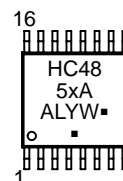
SOIC-16  
D SUFFIX  
CASE 751B



SOIC-16 WIDE  
DW SUFFIX  
CASE 751G



TSSOP-16  
DT SUFFIX  
CASE 948F



x = 1 or 2  
A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC4851A, MC74HC4852A

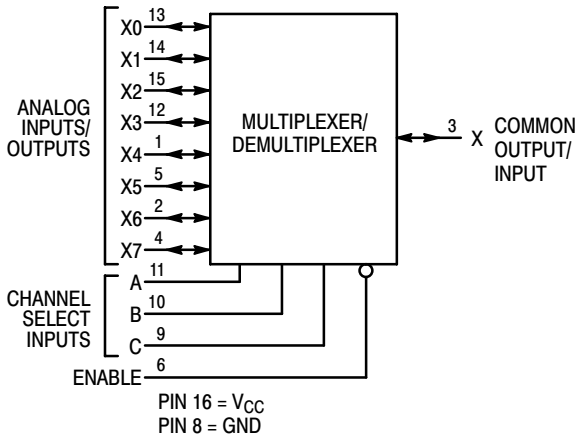


Figure 1. MC74HC4851A Logic Diagram Single-Pole, 8-Position Plus Common Off

FUNCTION TABLE – MC74HC4851A

Control Inputs			ON Channels	
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

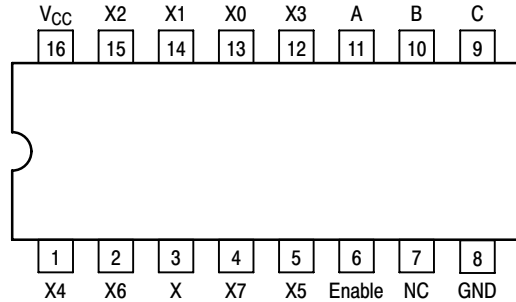


Figure 2. MC74HC4851A 16-Lead Pinout (Top View)

FUNCTION TABLE – MC74HC4852A

Control Inputs			ON Channels	
Enable	Select		Y0	X0
	B	A		
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

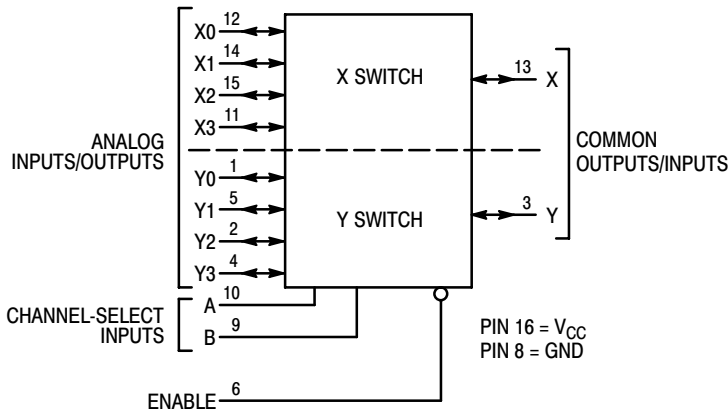


Figure 3. MC74HC4852A Logic Diagram Double-Pole, 4-Position Plus Common Off

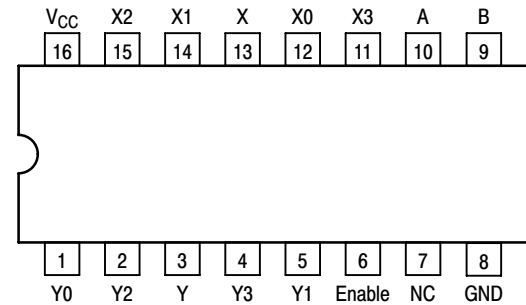


Figure 4. MC74HC4852A 16-Lead Pinout (Top View)

# MC74HC4851A, MC74HC4852A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	-0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Any Pin) (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	$\pm 25$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
$T_{stg}$	Storage Temperature Range	-65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}$	DC Input Voltage (Any Pin) (Referenced to GND)	GND	$V_{CC}$	V
$V_{IO}^*$	Static or Dynamic Voltage Across Switch	0.0	1.2	V
$T_A$	Operating Temperature Range, All Package Types	- 55	+ 125	°C
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

\*For voltage drops across switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = GND$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
$I_{in}$	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	$V_{in} = V_{CC} \text{ or } GND$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in(\text{digital})} = V_{CC} \text{ or } GND$ $V_{in(\text{analog})} = GND$	6.0	2	20	40	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# MC74HC4851A, MC74HC4852A

## DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V <sub>CC</sub>	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> to GND; I <sub>S</sub> ≤ 2.0 mA	2.0	1700	1750	1800	Ω
			3.0	1100	1200	1300	
			4.5	550	650	750	
			6.0	400	500	600	
ΔR <sub>on</sub>	Delta "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; V <sub>IS</sub> = V <sub>CC</sub> /2 I <sub>S</sub> ≤ 2.0 mA	2.0	300	400	500	Ω
			3.0	160	200	240	
			4.5	80	100	120	
			6.0	60	80	100	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel  Common Channel	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1 ±0.2	±0.5 ±2.0	±1.0 ±4.0	μA
I <sub>on</sub>	Maximum On-Channel Leakage Channel-to-Channel	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.2	±2.0	±4.0	μA

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

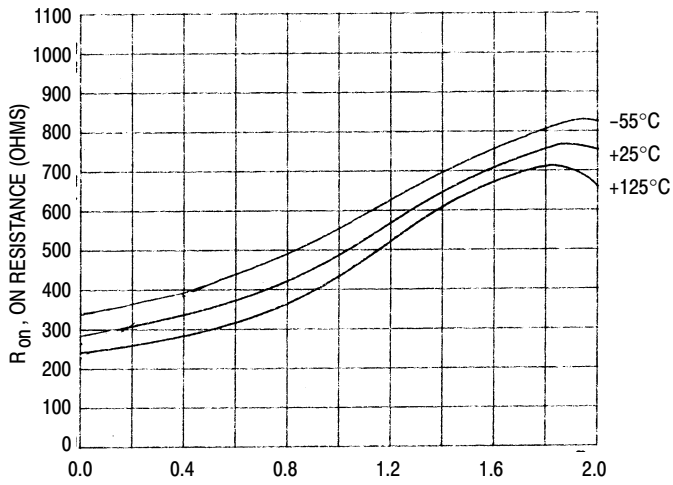
Symbol	Parameter	V <sub>CC</sub>	-55 to 25°C	≤85°C	≤125°C	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Analog Input to Analog Output	2.0	160	180	200	ns
		3.0	80	90	100	
		4.5	40	45	50	
		6.0	30	35	40	
t <sub>PHL</sub> , t <sub>PHZ,PZH</sub> , t <sub>PLH</sub> , t <sub>PLZ,PZL</sub>	Maximum Propagation Delay, Enable or Channel-Select to Analog Output	2.0	260	280	300	ns
		3.0	160	180	200	
		4.5	80	90	100	
		6.0	60	70	80	
C <sub>in</sub>	Maximum Input Capacitance (All Switches Off) Any Single Analog Pin (All Switches Off) Common Analog Pin		10	10	10	pF
			35	35	35	
			130	130	130	
C <sub>PD</sub>	Power Dissipation Capacitance	Typical	5.0	20		pF

## INJECTION CURRENT COUPLING SPECIFICATIONS (V<sub>CC</sub> = 5V, T<sub>A</sub> = -55°C to +125°C)

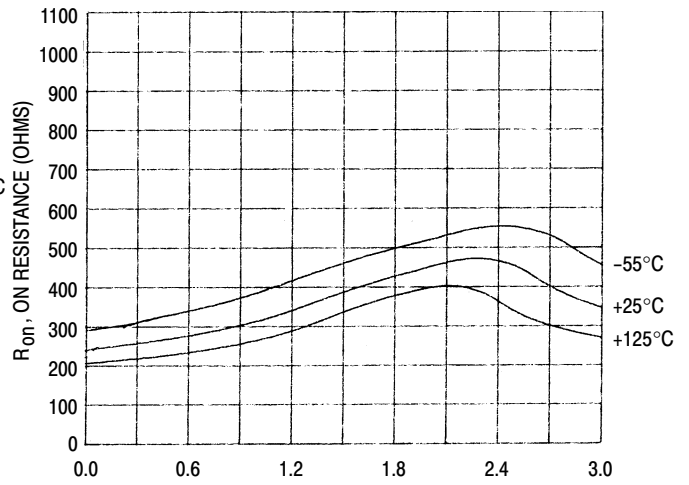
Symbol	Parameter	Condition	Typ	Max	Unit
VΔ <sub>out</sub>	Maximum Shift of Output Voltage of Enabled Analog Channel	I <sub>in</sub> * ≤ 1 mA, R <sub>S</sub> ≤ 3,9 kΩ	0.1	1.0	mV
		I <sub>in</sub> * ≤ 10 mA, R <sub>S</sub> ≤ 3,9 kΩ	1.0	5.0	
		I <sub>in</sub> * ≤ 1 mA, R <sub>S</sub> ≤ 20 kΩ	0.5	2.0	
		I <sub>in</sub> * ≤ 10 mA, R <sub>S</sub> ≤ 20 kΩ	5.0	20	

\* I<sub>in</sub> = Total current injected into all disabled channels.

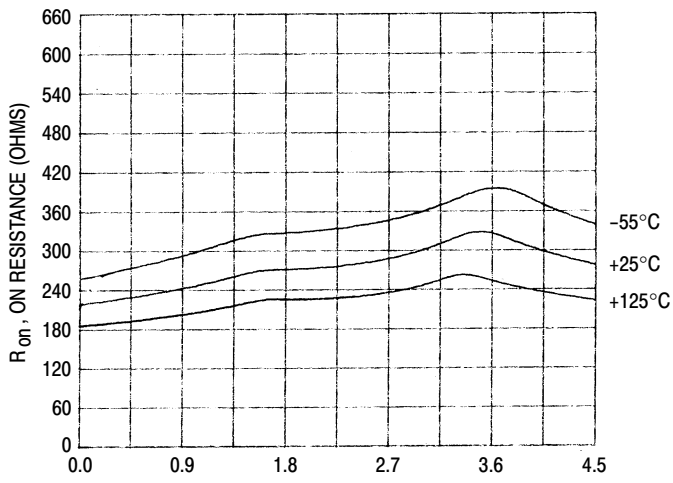
# MC74HC4851A, MC74HC4852A



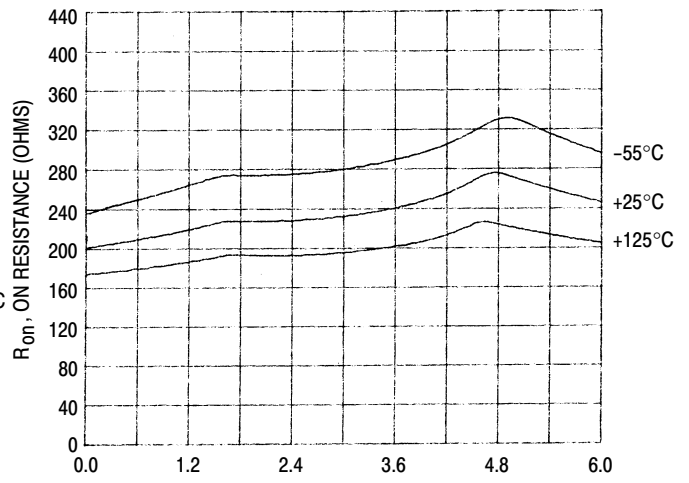
$V_{in}$ , INPUT VOLTAGE (VOLTS), REFERENCED TO GND  
**Figure 5. Typical On Resistance  $V_{CC} = 2V$**



$V_{in}$ , INPUT VOLTAGE (VOLTS), REFERENCED TO GND  
**Figure 6. Typical On Resistance  $V_{CC} = 3V$**

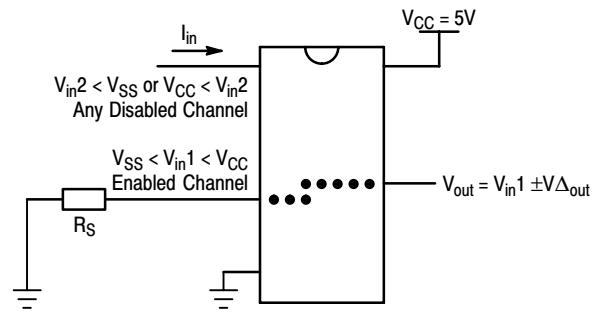


$V_{in}$ , INPUT VOLTAGE (VOLTS), REFERENCED TO GND  
**Figure 7. Typical On Resistance  $V_{CC} = 4.5V$**

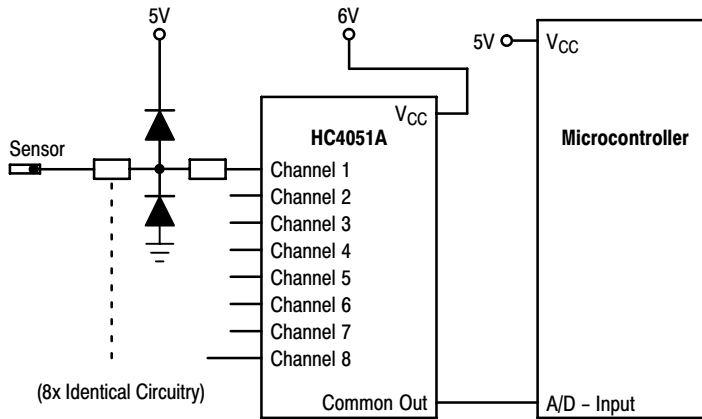


$V_{in}$ , INPUT VOLTAGE (VOLTS), REFERENCED TO GND  
**Figure 8. Typical On Resistance  $V_{CC} = 6V$**

# MC74HC4851A, MC74HC4852A

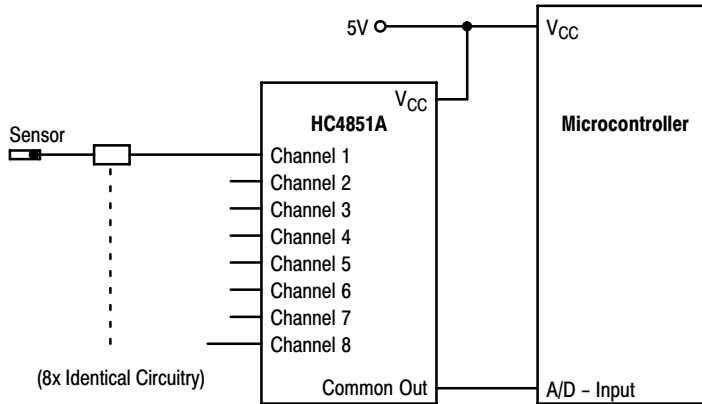


**Figure 9. Injection Current Coupling Specification**



**Figure 10. Actual Technology**

Requires 32 passive components and one extra 6V regulator to suppress injection current into a standard HC4051 multiplexer



**Figure 11. MC74HC4851A Solution**

Solution by applying the HC4851A multiplexer

# MC74HC4851A, MC74HC4852A

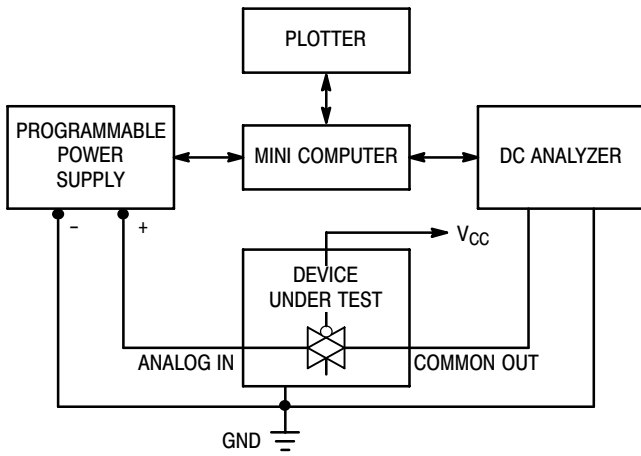


Figure 12. On Resistance Test Set-Up

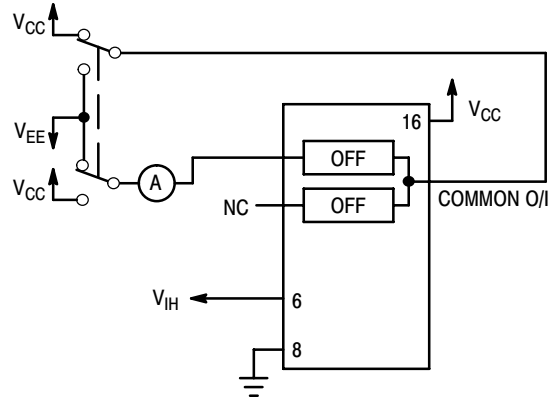


Figure 13. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

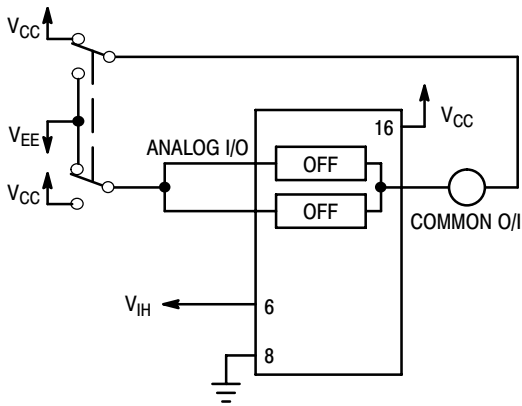


Figure 14. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

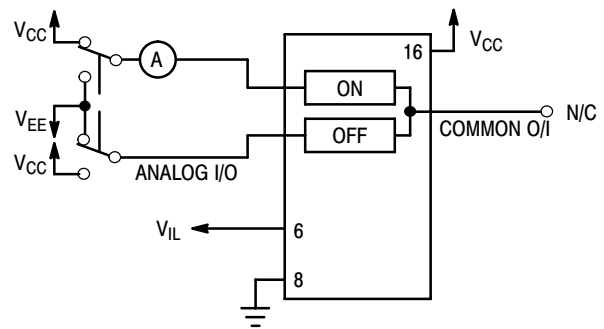


Figure 15. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

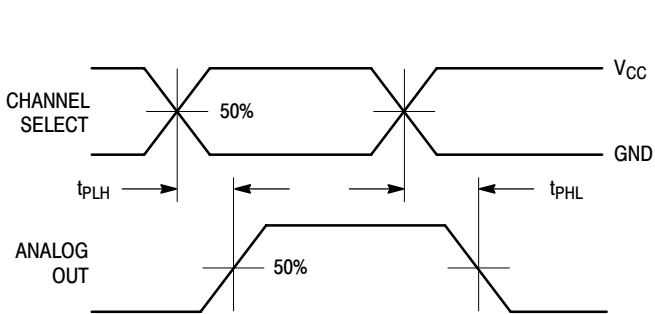
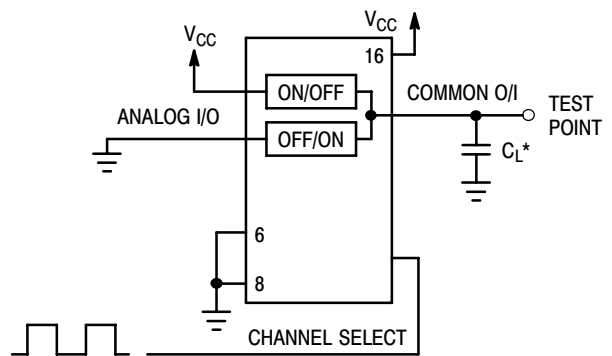


Figure 16. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance

Figure 17. Propagation Delay, Test Set-Up Channel Select to Analog Out

MC74HC4851A, MC74HC4852A

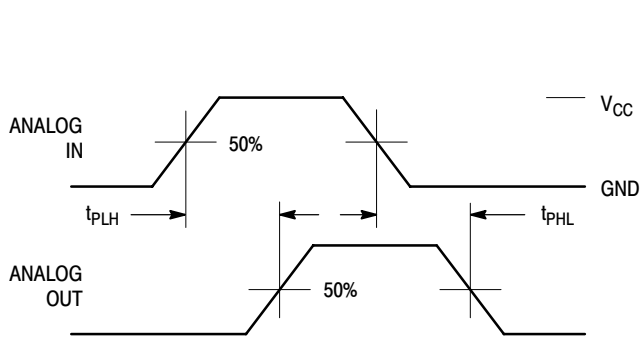
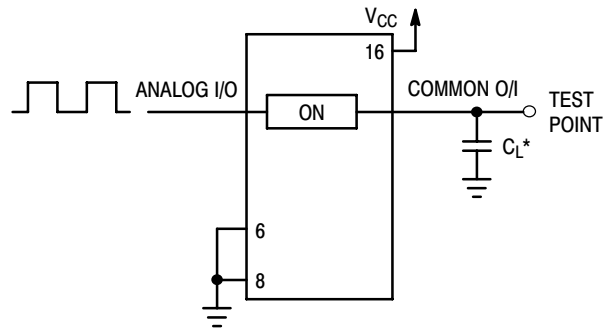


Figure 18. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance

Figure 19. Propagation Delay, Test Set-Up Analog In to Analog Out

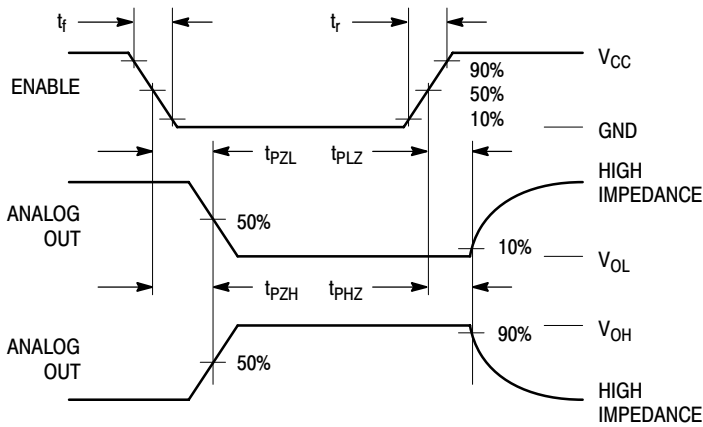


Figure 20. Propagation Delays, Enable to Analog Out

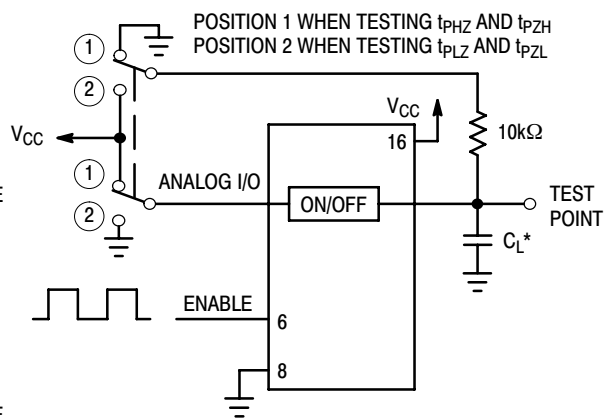


Figure 21. Propagation Delay, Test Set-Up Enable to Analog Out

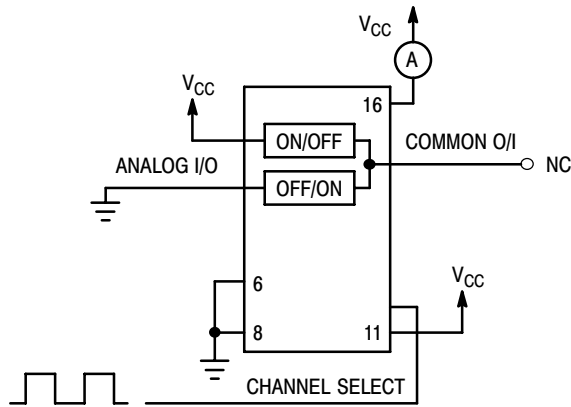
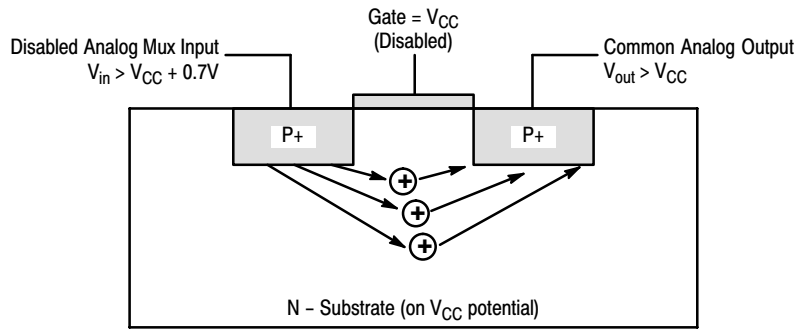


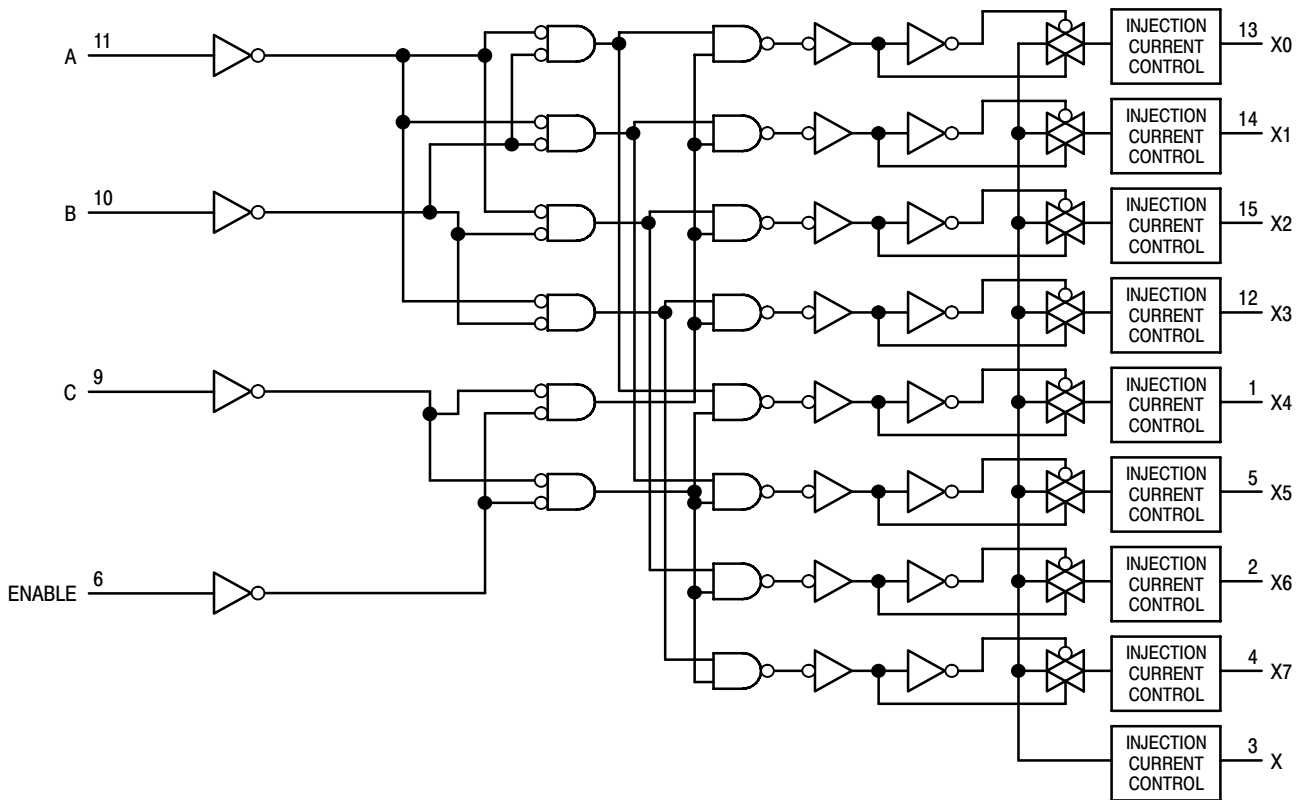
Figure 22. Power Dissipation Capacitance, Test Set-Up



# MC74HC4851A, MC74HC4852A



**Figure 23. Diagram of Bipolar Coupling Mechanism**  
 Appears if  $V_{in}$  exceeds  $V_{CC}$ , driving injection current into the substrate



**Figure 24. Function Diagram, HC4851A**

# MC74HC4851A, MC74HC4852A

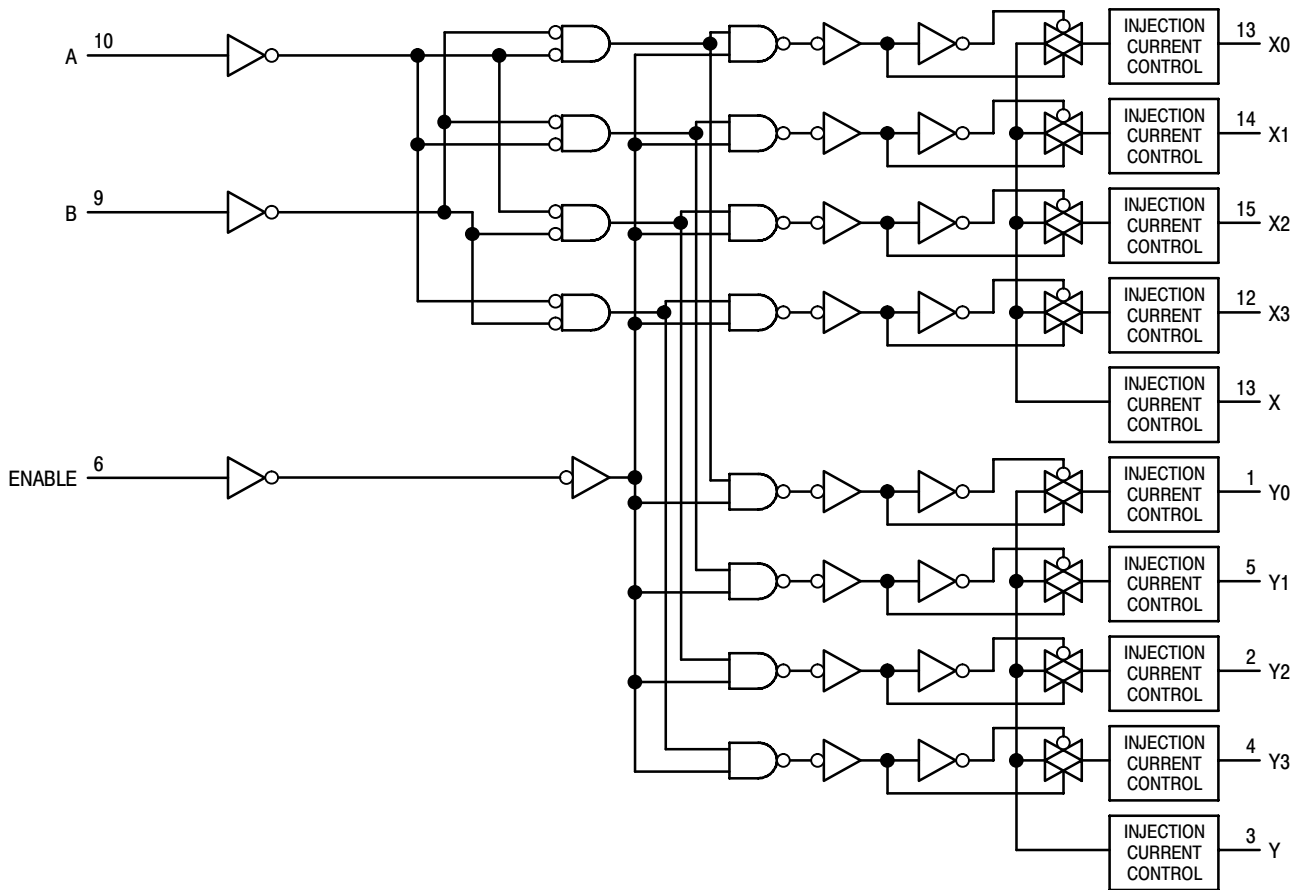


Figure 25. Function Diagram, HC4852A

## MC74HC4851A, MC74HC4852A

### ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4851AN	PDIP-16	500 Units / Box
MC74HC4851ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HC4851AD	SOIC-16	48 Units / Rail
MC74HC4851ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4851ADR2	SOIC-16	2500 Units / Tape & Reel
MC74HC4851ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC74HC4851ADTR2	TSSOP-16*	2500 Units / Tape & Reel
MC74HC4851ADTR2G	TSSOP-16*	2500 Units / Tape & Reel
MC74HC4851ADW	SOIC-16 WIDE	48 Units / Rail
MC74HC4851ADWG	SOIC-16 WIDE (Pb-Free)	48 Units / Rail
MC74HC4851ADWR2	SOIC-16 WIDE	1000 Units / Tape & Reel
MC74HC4851ADWR2G	SOIC-16 WIDE (Pb-Free)	1000 Units / Tape & Reel
MC74HC4852AN	PDIP-16	500 Units / Box
MC74HC4852ANG	PDIP-16 (Pb-Free)	500 Units / Box
MC74HC4852AD	SOIC-16	48 Units / Rail
MC74HC4852ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4852ADR2	SOIC-16	2500 Units / Tape & Reel
MC74HC4852ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC74HC4852ADTR2	TSSOP-16*	2500 Units / Tape & Reel
MC74HC4852ADTR2G	TSSOP-16*	2500 Units / Tape & Reel

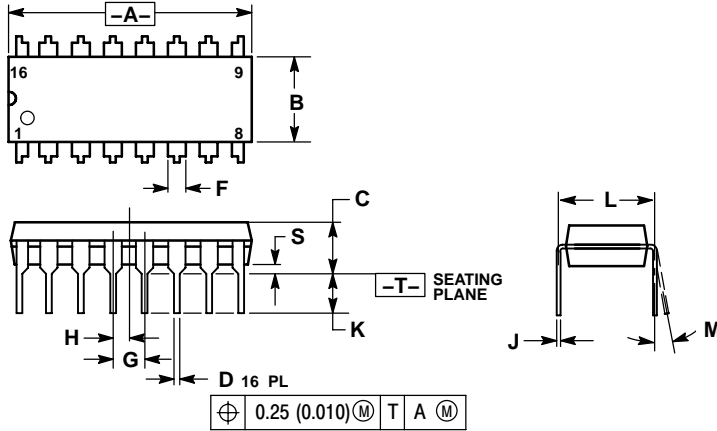
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HC4851A, MC74HC4852A

## PACKAGE DIMENSIONS

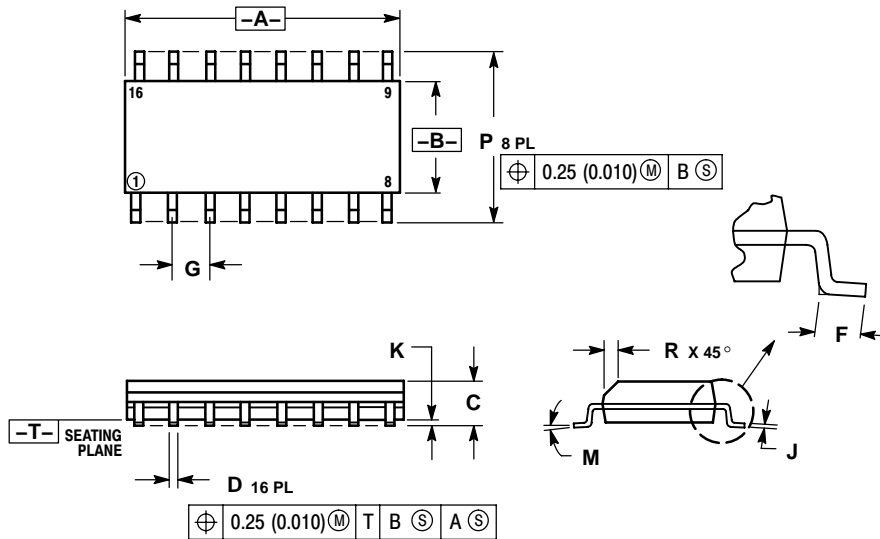
PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°		10°	
S	0.020	0.040	0.51	1.01

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J

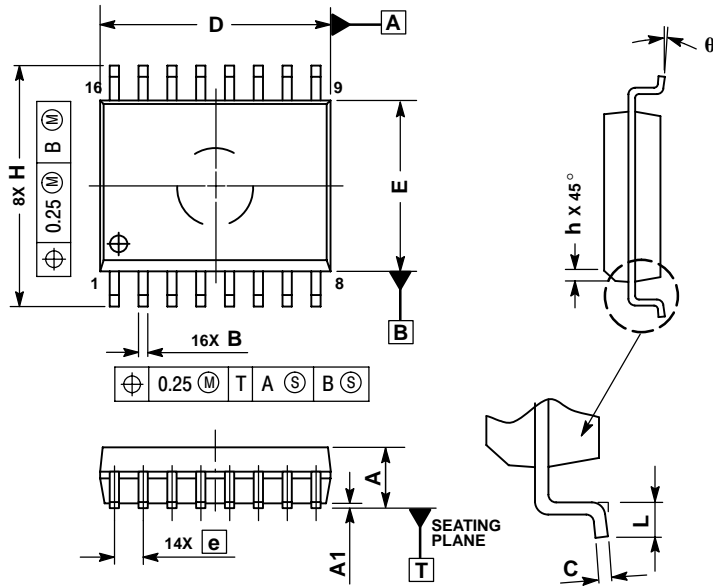


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°		7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# MC74HC4851A, MC74HC4852A

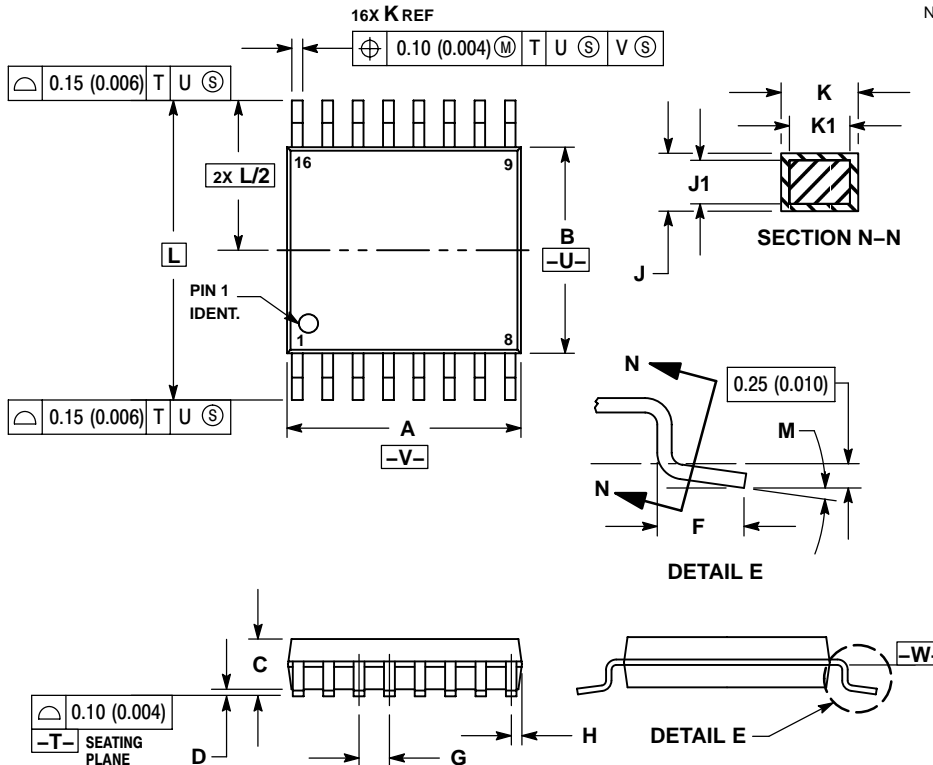
SOIC-16 WIDE  
DW SUFFIX  
CASE 751G-03  
ISSUE C



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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