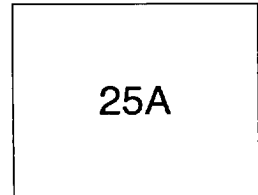


### PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

#### Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200  $V_{RRM}$ ,  $V_{DRM}$
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved



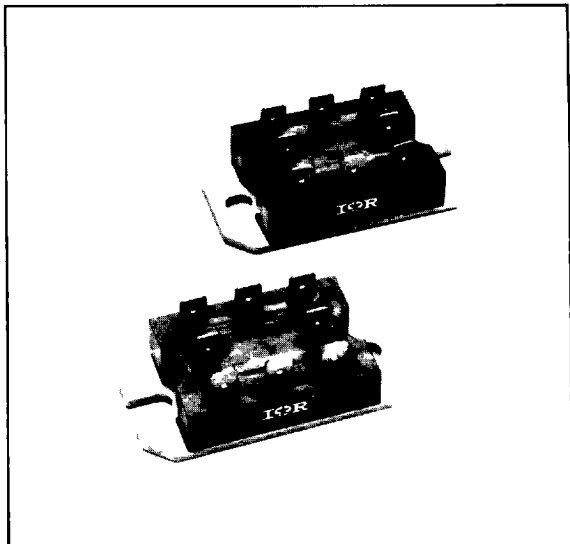
#### Description

The P100 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

#### Major Ratings and Characteristics

Parameters	P100	Units
$I_D$	25	A
@ $T_C$	85	°C
$I_{FSM}$ @ 50Hz	357	A
@ 60Hz	375	A
$I^2t$ @ 50Hz	637	A <sup>2</sup> s
@ 60Hz	580	A <sup>2</sup> s
$I^2t$	6365	A <sup>2</sup> s
$V_{RRM}$ range	400 to 1200	V
$V_{INS}$	2500	V
$T_J$	-40 to 125	°C



## ELECTRICAL SPECIFICATIONS

## Voltage Ratings

Type number	$V_{RRM}$ maximum repetitive peak reverse voltage V	$V_{RSM}$ maximum non-repetitive peak reverse voltage V	$V_{DRM}$ maximum repetitive peak off-state voltage V
P101, P111, P121, P131, P141, P161, P171	400	500	400
P102, P112, P122, P132, P142, P162, P172	600	700	600
P103, P113, P123, P133, P143, P163, P173	800	900	800
P104, P114, P124, P134, P144, P164, P174	1000	1100	1000
P105, P115, P125, P135, P145, P165, P175	1200	1300	1200

## On-state Conduction

Parameters	P100	Units	Conditions		
$I_D$ Maximum DC output Current	25	A	@ $T_C = 85^\circ\text{C}$ , full bridge circuits 0,1,2 and 3		
$I_{T(AV)}$ Maximum average on-state and forward current $I_{F(AV)}$	12.5	A	180° sine conduction circuits 6, 7		
$I_{RMS}$ Maximum RMS current	28	A	180° sine conduction circuit 4		
$I_{TSM}$ Maximum peak one-cycle non repetitive on-state or forward current $I_{FSM}$	357	A	10ms	No voltage	Sinusoidal half Wave Initial $T_J = T_{J,max}$
	375	A	8.3ms	reapplied	
	300	A	10ms	100% $V_{RRM}$	Sinusoidal half Wave Initial $T_J = T_{J,max}$
	315	A	8.3ms	reapplied	
$I^2t$ Maximum $I^2t$ for fusing	637	A <sup>2</sup> s	10ms	No voltage	Initial $T_J = T_{J,max}$
	580	A <sup>2</sup> s	8.3ms	reapplied	
	450	A <sup>2</sup> s	10ms	100% voltage	Initial $T_J = T_{J,max}$
	410	A <sup>2</sup> s	8.3ms	reapplied	
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	6365	A <sup>2</sup> $\sqrt{s}$	t=0 to 10ms, no voltage reapplied $I^2t$ for time tx = $I^2\sqrt{t} \sqrt{tx}$		
$V_{T(TO)}$ Maximum value of threshold voltage	0.82	V	$T_J = 125^\circ\text{C}$		
$r_t$ Maximum value of on-state or forward slope resistance	12	m $\Omega$	$T_J = 125^\circ\text{C}$ , Av. power = $V_{T(TO)} \cdot I_{T(AV)} + r_t \cdot (I_{T(RSM)})^2$		
$V_{TM}$ Maximum peak on-state or forward voltage drop $V_{FM}$	1.35	V	$T_J = 25^\circ\text{C}$ $I_{TM} = \pi \times I_{T(AV)}$		
	1.35	V	$T_J = 25^\circ\text{C}$ $I_{FM} = \pi \times I_{F(AV)}$		
$di/dt$ Maximum non repetitive rate of rise of turned on current	200	A/ $\mu\text{s}$	$T_J = 125^\circ\text{C}$ from 0.67 $V_{DRM}$ $I_{TM} = \pi \times I_{T(AV)}$ , $I_g = 500\text{mA}$ , tr < 0.5 $\mu\text{s}$ , tp > 6 $\mu\text{s}$		
$I_H$ Maximum holding current	100	mA	$T_J = 25^\circ\text{C}$ anode supply=6V, resistive load, gate open		
$I_L$ Maximum latching current	250	mA	$T_J = 25^\circ\text{C}$ anode supply=6V, resistive load		

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Blocking

Parameters	P100	Units	Conditions
$dv/dt$ Maximum critical rate of rise of off-state voltage	200	V/ $\mu$ s	$T_J = 125^\circ\text{C}$ , exponential to $0.67 V_{DRM}$ gate open
$I_{RRM}$ Maximum peak reverse and off-state leakage current at $V_{RRM}, V_{DRM}$	10	mA	$T_J = 125^\circ\text{C}$ , gate open circuit
$I_{RRM}$ Max. peak reverse leakage current	100	$\mu$ A	$T_J = 25^\circ\text{C}$
$V_{INS}$ RMS isolation voltage	2500	V	50Hz, circuit to base, all terminals shorted $T_J = 25^\circ\text{C}, t = 1 \text{ s}$

Triggering

Parameters	P100	Units	Conditions
$P_{GM}$ Maximum peak gate power	8.0	W	
$P_{G(AV)}$ Maximum average gate power	2.0	W	
$I_{GM}$ Maximum peak gate current	2.0	A	
$-V_{GM}$ Maximum peak negative gate voltage	10	V	
$V_{GT}$ Maximum gate voltage required to trigger	3.0	V	$T_J = -40^\circ\text{C}$
	2.0	V	$T_J = 25^\circ\text{C}$
	1.0	V	$T_J = 125^\circ\text{C}$
$I_{GT}$ Maximum gate current required to trigger	90	mA	$T_J = -40^\circ\text{C}$
	60	mA	$T_J = 25^\circ\text{C}$
	35	mA	$T_J = 125^\circ\text{C}$
$V_{GD}$ Maximum gate voltage that will not trigger	0.2	V	$T_J = 125^\circ\text{C}$ , rated $V_{DRM}$ applied
$I_{GD}$ Maximum gate current that will not trigger	2.0	mA	$T_J = 125^\circ\text{C}$ , rated $V_{DRM}$ applied

Thermal and Mechanical Specifications

Parameters	P100	Units	Conditions
$T_J$ Junction temperature range	-40 to 125	$^\circ\text{C}$	
$T_{stg}$ Storage temperature range	-40 to 150	$^\circ\text{C}$	
$R_{thJC}$ Maximum thermal resistance, junction to case	2.24	K/W	DC operation per junction
$R_{thc-S}$ Maximum thermal resistance	0.10	K/W	Mounting surface smooth and greased per module 0,1,2,3
	0.20	K/W	Mounting surface smooth and greased per module 4,6,7
T Mounting torque, base to heatsink $\pm 10\%$	4	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound.
wt Approximate weight	58 (2.0)	g (oz)	

Circuit Type and Coding

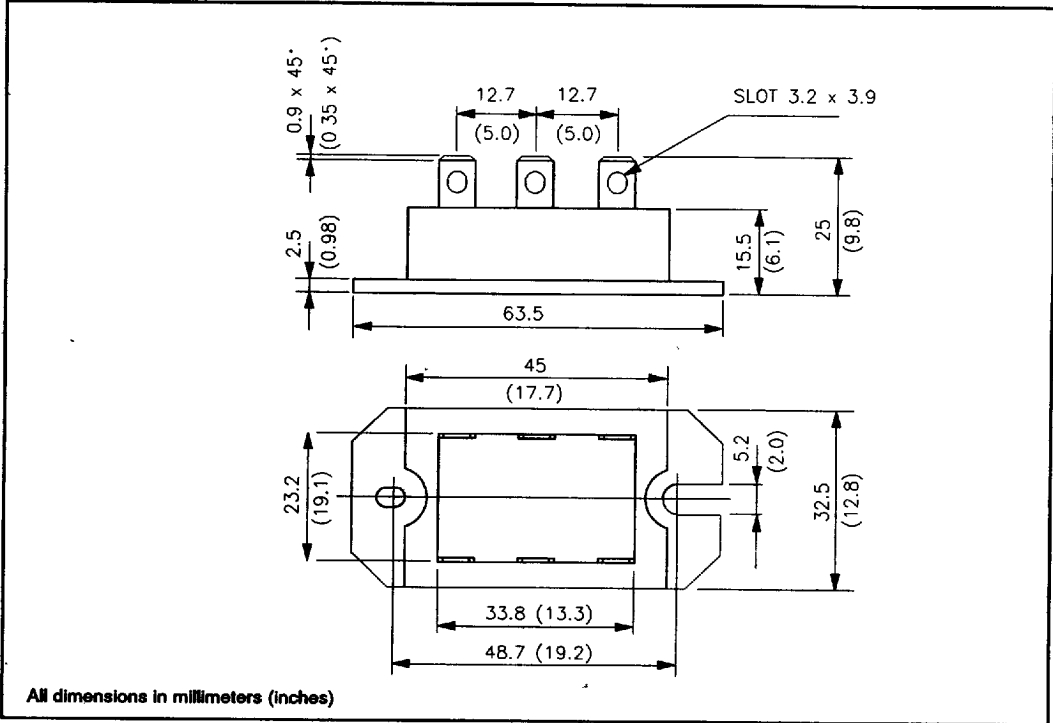
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	Circuit "0"	Circuit "1"	Circuit "2"	Circuit "3"	Circuit "4"	Circuit "6"	Circuit "7"
<b>Terminal Positions</b>							
<b>Schematic diagram</b>							
	Single Phase Hybrid Bridge Common Cathode	Single Phase Hybrid Bridge Common Anode	Single Phase Hybrid Bridge Doubler Connection	Single Phase AllSCR Bridge	SCR AC Switch	Hybrid Doubler	SCR Doubler
<b>Basic series</b>	P10.	P11.	P12.	P13.	P14.	P16.	P17.
<b>With voltage suppression</b>	P10.K	P11.K	P12.K	P13.K	P14.K	-	-
<b>With free-wheeling diode</b>	P10.W	P11.W	-	-	-	-	-
<b>With both voltage suppression and free-wheeling diode</b>	P10.KW	P11.KW	-	-	-	-	-

\* To complete code refer to voltage ratings table, i.e.: for 600V P110.W complete code is P102W

Outline Table



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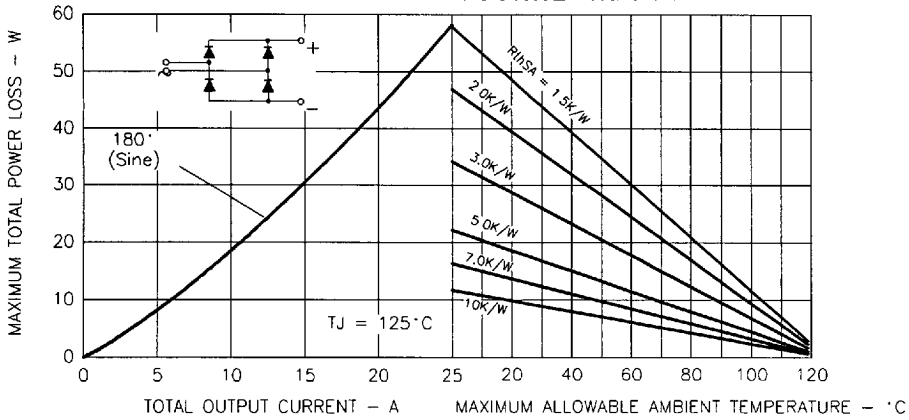


Fig. 1 - Current Rating Nomogram (1 Module Per Heatsink), Circuits '0', '1', '2', '3'

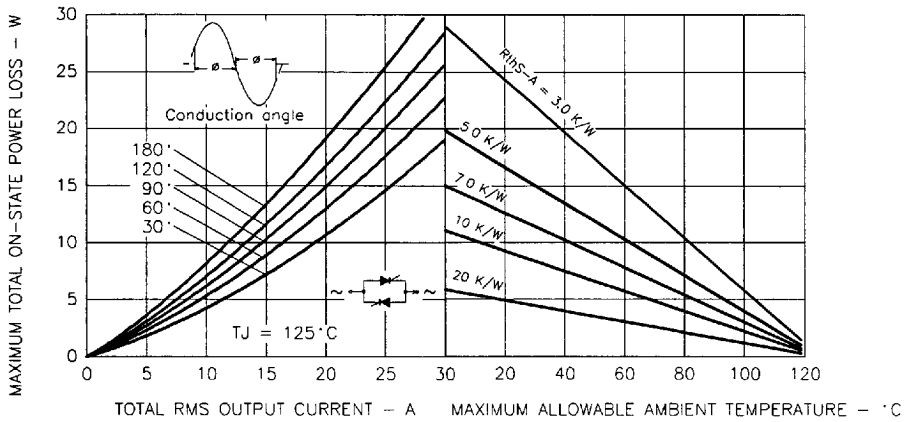


Fig. 2 - Current Rating Nomogram (1 Module Per Heatsink), Circuit '4'

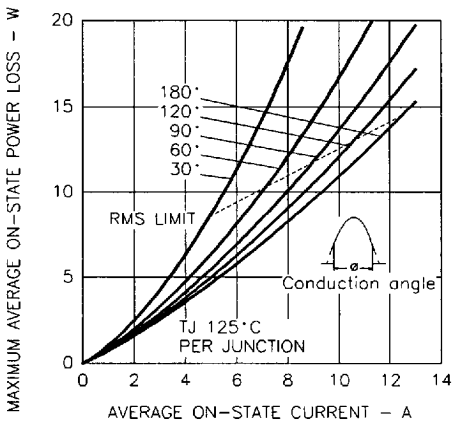


Fig. 3 - On-state Power Loss Characteristics

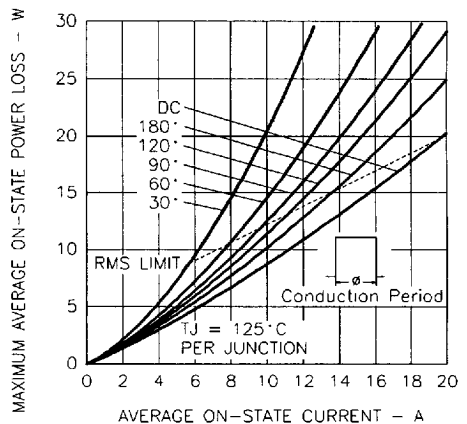


Fig. 4 - On-state Power Loss Characteristics



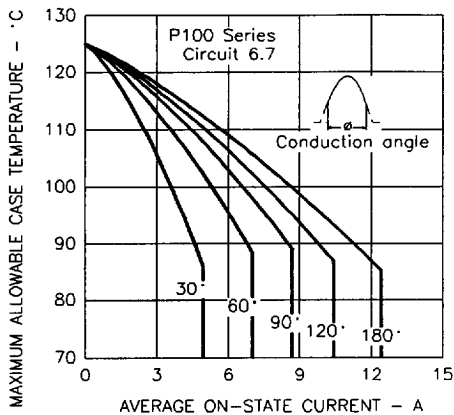


Fig. 5 - Current Ratings Characteristics

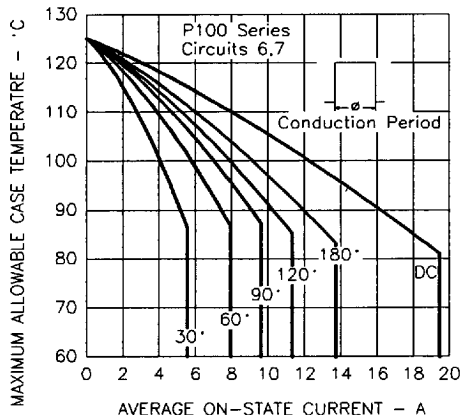


Fig. 6 - Current Ratings Characteristics

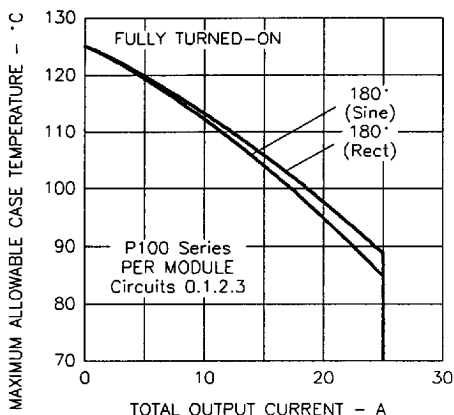


Fig. 7 - Current Ratings Characteristics

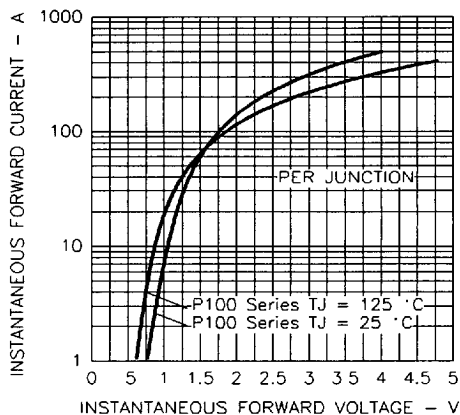


Fig. 8 - On-state Voltage Drop Characteristics

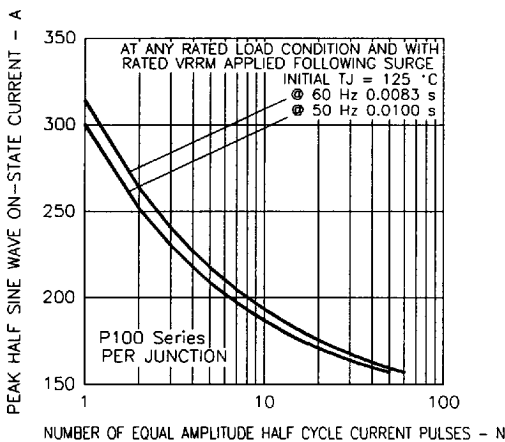


Fig. 9 - Maximum Non-Repetitive Surge Current

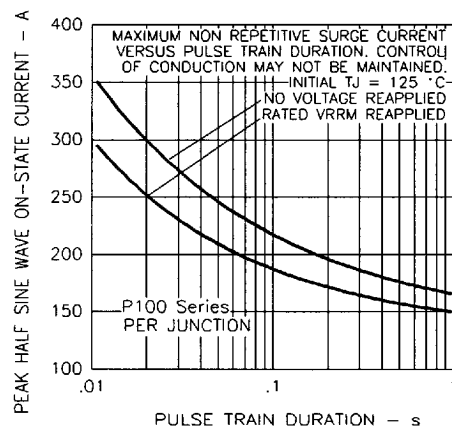


Fig. 10 - Maximum Non-Repetitive Surge Current

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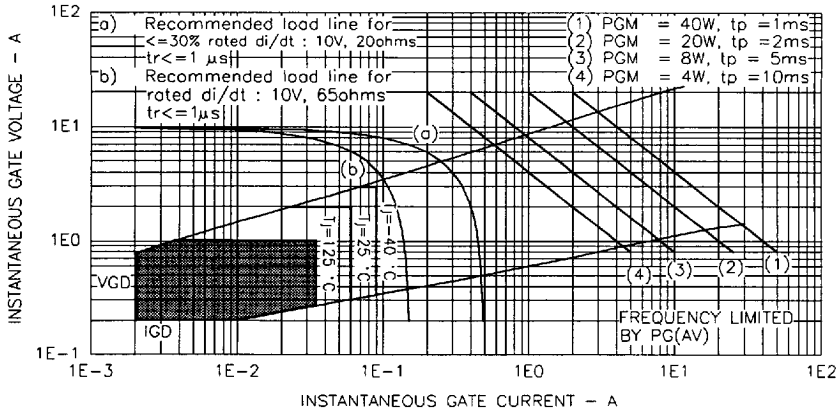


Fig. 11 - Gate Characteristics

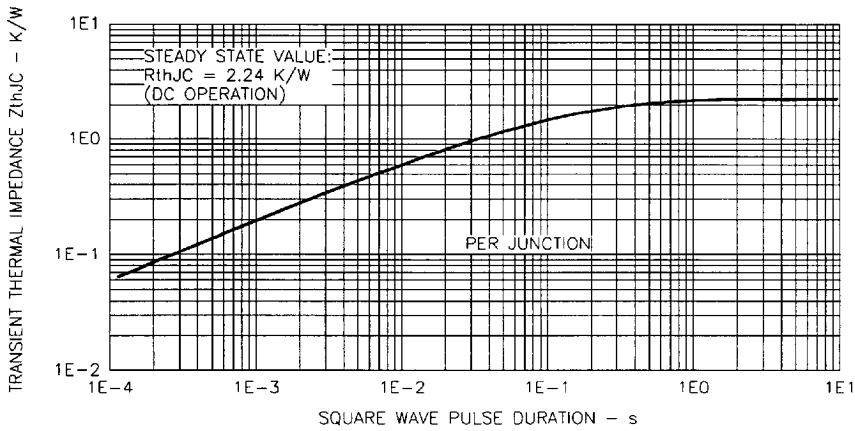


Fig. 12 - Thermal Impedance  $Z_{thJC}$  Characteristics

