WESTCODE SEMICONDUCTORS

Technical Publication
TR216C
Issue 2
May 1985

High Frequency Inverter Grade Capsule Thyristor Type R216C

distributed amplified gate for high di/dt and low switching losses

560 amperes average: up to 1200 volts V_{RRM}/V_{DRM}

Ratings (Maximum values at 125°C Tj unless stated otherwise)

RATING	CONDITIONS	SYMBOL	
Average on-state current	Half sine wave, 55°C heatsink temperature (double side cooled)	$I_{T(AV)}$	560 A
	Half sine wave, 85°C heatsink temperature (single side cooled)		215 A
R.M.S. on-state current	25°C heatsink temperature, double side cooled	$I_{T(RMS)}$	1125 A
Continuous on-state current	25°C heatsink temperature, double side cooled	I_T	925 A
Peak one-cycle surge (non-repetitive) on state current	10ms duration, 60% V_{RRM} re-applied	$I_{TSM(1)}$	6300 A
	10ms duration, $V_R \leq$ 10 volts	$I_{TSM(2)}$	6900 A
Maximum permissible surge energy	10ms duration, $V_R \leq$ 10 volts	I^2t	240×10^3 A^2s
	3ms duration, $V_R \leq$ 10 volts	I^2t	180×10^3 A^2s
Peak forward gate current	Anode positive with respect to cathode	I_{FGM}	11 A
Peak forward gate voltage	Anode positive with respect to cathode	V_{FGM}	13.5 V
Peak reverse gate voltage		V_{RGM}	5 V
Average gate power		P_G	1.5 W
Peak gate power	100μs. pulse width	P_{GM}	60 W
Rate of rise of off-state voltage	To 80% V_{DRM} gate open-circuit	dv/dt	*200 V/μs
Rate of rise of on-state current (repetitive)	Gate drive 20 volts, 20 ohms with $t_r \leq 1\mu s$. Anode voltage ≤ 80% V_{DRM}	di/dt (1)	500 A/μs
Rate of rise of on-state current (non-repetitive)		di/dt (2)	1000 A/μs
Operating temperature range		T_{hs}	−40 + 125°C
Storage temperature range		T_{stg}	−40 + 150°C

Characteristics (Maximum values at 125°C Tj unless stated otherwise)

CHARACTERISTIC	CONDITIONS	SYMBOL	
Peak on-state voltage	At 1000 A, I_{TM}	V_{TM}	1.85 V
Forward conduction threshold voltage		V_O	1.23 V
Forward conduction slope resistance		r	0.62 mΩ
Repetitive peak off-state current	At V_{DRM}	I_{DRM}	60 mA
Repetitive peak reverse current	At V_{RRM}	I_{RRM}	60 mA
Maximum gate current required to fire all devices	At 25°C, V_A = 6 V, I_A = 1A	I_{GT}	200 mA
Maximum gate voltage required to fire all devices		V_{GT}	3 V
Maximum holding current		I_H	1 A
Maximum gate voltage which will not trigger any device		V_{GD}	0.25 V
Stored charge	I_{TM} = 550 A, dir/dt 40 A/μs, V_{RM} = 50V, 50% chord value	Q_{rr}	85 μC
Circuit commutated turn-off time available down to	I_{TM} = 550 A, dir/dt = 40A/μs, V_{RM} = 50V, 200V/μs to 80% V_{DRM}	tq	20–30 μs
	20V/μs to 80% V_{DRM}	tq typical	10–25 μs
Thermal resistance, junction to heat sink, for a device with a maximum forward volt drop characteristic	Double side cooled	$R_{th(j-hs)}$	0.06°C/W
	Single side cooled		0.12°C/W

VOLTAGE CODE		H02	H04	H06	H08	H10	H12		
Repetitive peak voltages Non-repetitive peak off-state voltage	V_{RRM} V_{DRM} V_{DSM}	200	400	600	800	1000	1200		
Non-repetitive peak reverse blocking voltage	V_{RSM}	300	500	700	900	1100	1300		

Ordering Information (Please quote device code as explained below — 11 digits)

R 2 1 6 C	● ● ●	●	●	0
Fixed type code	Voltage Code (see ratings)	dv/dt code to 80% V_{DRM} C = 20V/μs E = 100V/μs D = 50V/μs F = 200V/μs	Turn-off time H = 30 μs J = 25 μs K = 20 μs L = 15 μs N = 10 μs	

Typical code: R216CH08FJ0 = 800 V_{RRM} 800 V_{DRM} 200 V/μs dv/dt to 80% V_{DRM} 25 μs turn-off

*Other values of dv/dt up to 1000 V/μs, and turn-off time may be available.

1. INTRODUCTION

The R216C thyristor series incorporates diffused silicon slices 30 mm diameter in cold-weld housings. Fast turn-on is achieved by interdigitation of the cathode, enabling these devices to withstand high di/dt and give low turn-on loss in chopper and inverter operation.

2. NOTES ON THE RATINGS

(a) **Rate of rise of on-state current**
The maximum un-primed rate of rise of on-state current must not exceed 1000 A/μs at any time during turn-on on a non-repetitive basis. For repetitive performance the on-state rate of rise of current must not exceed 500 A/μs at any time during turn-on. Note that these values of current rate of rise apply to the circuit external to the device and its specified snubber network and device current rates of rise will be higher.

(b) **Square wave ratings**
These ratings are given for leading edge linear rates of rise of forward current of 100 and 500 A/μs.

(c) **Duty Cycle Lines**
The 100% duty cycle line appears on all these ratings. These frequency ratings are presented in the form that all duty cycles may be represented by straight parallel lines.

(d) **Maximum operating Frequency**
The maximum operating frequency, f_{max}, is set by the time required for the thyristor to turn off (tq) and for the off-state voltage to reach full value (tv), i.e.

$$f_{max} = \frac{1}{t_{pulse} + tq + tv}$$

(e) **Energy per pulse characteristics**
These curves enable rapid estimation of device dissipation to be obtained for conditions not covered by the frequency ratings.

Let E_p be the Energy per pulse for a given current and pulse width, in joules.

Then $W_{AV} = E_p \times f$.

3. REVERSE RECOVERY LOSS

On account of the number of circuit variables affecting reverse recovery voltage, no allowance for reverse recovery loss has been made in these ratings. The following procedure is recommended for use where it is necessary to include reverse recovery loss.

(a) **Determination by Measurement**
From waveforms of recovery current obtained from a high frequency shunt (see Note 1) and reverse voltage present during recovery, an instantaneous reverse recovery loss waveform must be constructed. Let the area under this waveform be A joules per pulse. A new heat sink temperature can then be evaluated from:

$$T_{SINK}\ (new) = T_{SINK}\ (original) - A\left(\frac{r_t.10^6}{t} + R_{th} \times f\right)$$

where $r_t = 1.23 \times 10^{-4}\sqrt{t}$

t = duration of reverse recovery loss per pulse in microseconds

A = Area under reverse loss waveform per pulse in joules (W.S.)

f = rated frequency at the original heat sink temperature

The total dissipation is now given by

$W_{(TOT)} = W_{(original)} + A \times f$

(b) **Design Method**
In circumstances where it is not possible to measure voltage and current conditions, or for design purposes, the additional losses may be estimated from figure 7. A typical R-C snubber network is connected across the thyristor to control the transient reverse voltage waveform.

Let E be the value of energy per reverse cycle in joules (figure 7).

Let f be the operating frequency in Hz

then T_{SINK} new $= T_{SINK}$ original $- ER_{th} \times f$

where T_{SINK} new is the required maximum heat sink temperature

and T_{SINK} original is the heat sink temperature given with the frequency ratings.

4. GATE DRIVE

The recommended gate drive is 20 V, 20 ohms with a short-circuit current rise time of not more than 1 μs. This gate drive must be applied when using the full di/dt capability of the device.

5. THE DV/DT SUPPRESSION NETWORK

The effect of a conventional resistor-capacitor snubber of 0.22 μF 5 ohms has been included in these ratings and all rating di/dt values apply to the circuit external to the thyristor and its suppression network.

Snubber Network Values
A series connected C-R filter may be required across the anode to cathode terminals of the thyristor for the purpose of reducing off-state voltage overshoot.

The optimum values for C and R depend partly on the circuits connected to the thyristor. For most applications the snubber design values should not exceed a maximum of 0.22 μF or a minimum of 5 ohms. Please consult Westcode for values outside these limits.

6. NOTE 1

REVERSE RECOVERY LOSS BY MEASUREMENT

This thyristor has a low reverse recovered charge and peak reverse recovery current. When measuring the charge care must be taken to ensure that:

(a) a.c. coupled devices such as current transformers are not affected by prior passage of high amplitude forward current.

(b) The measuring oscilloscope has adequate dynamic range — typically 100 screen heights — to cope with the initial forward current without overload.

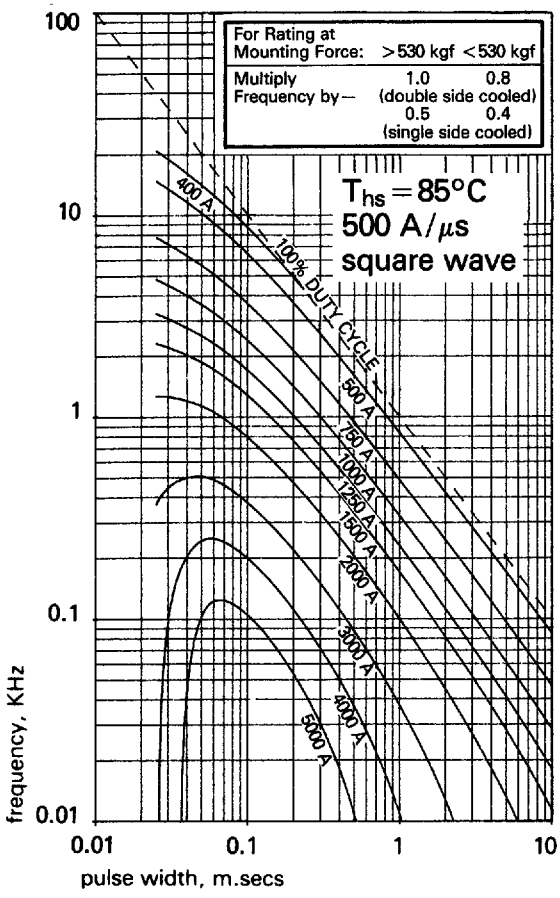


Figure 1 Frequency v. pulse width

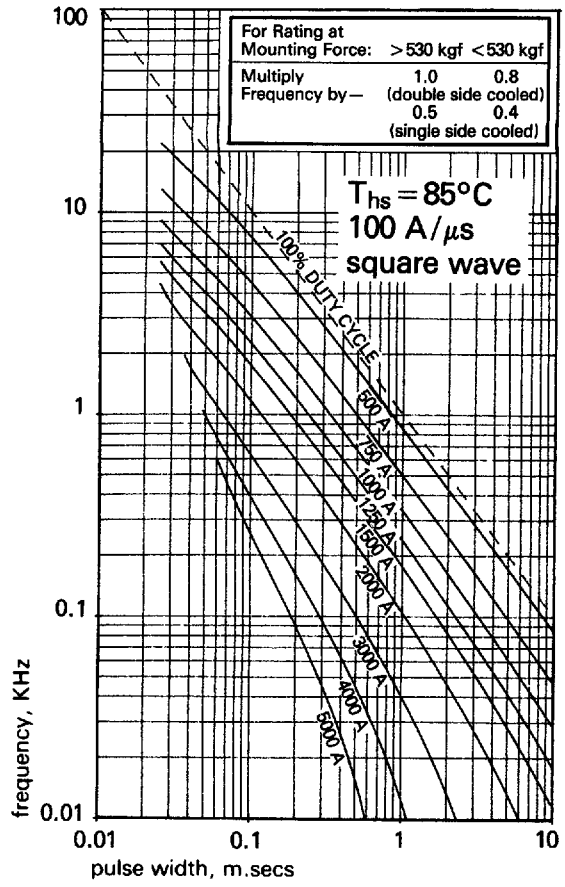


Figure 2 Frequency v. pulse width

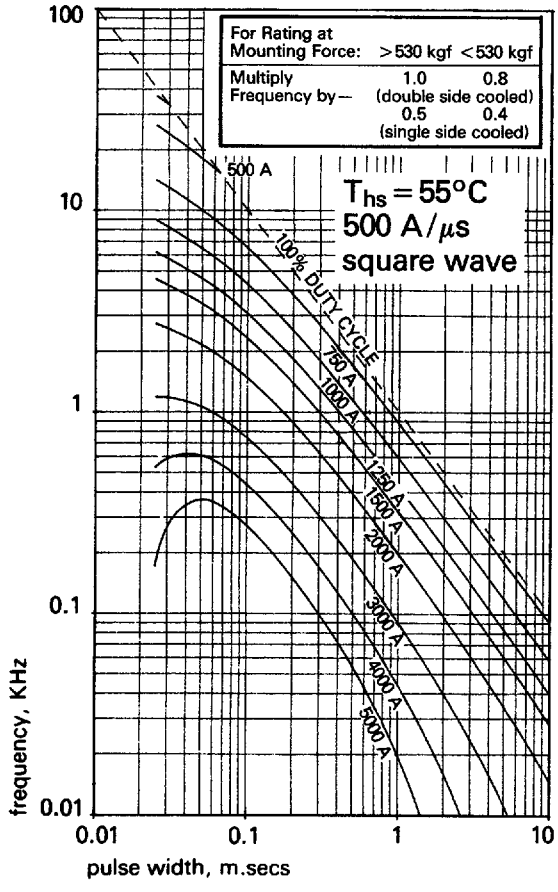


Figure 3 Frequency v. pulse width

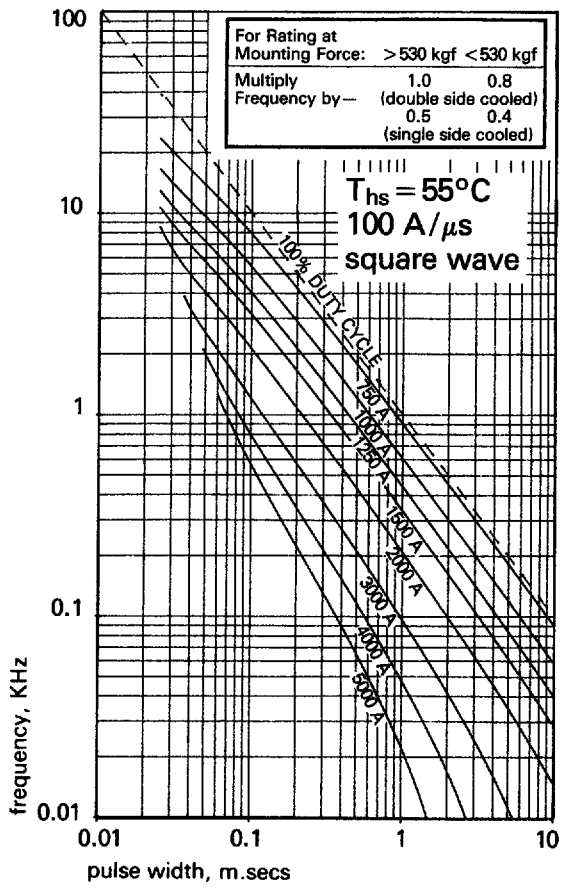


Figure 4 Frequency v. pulse width

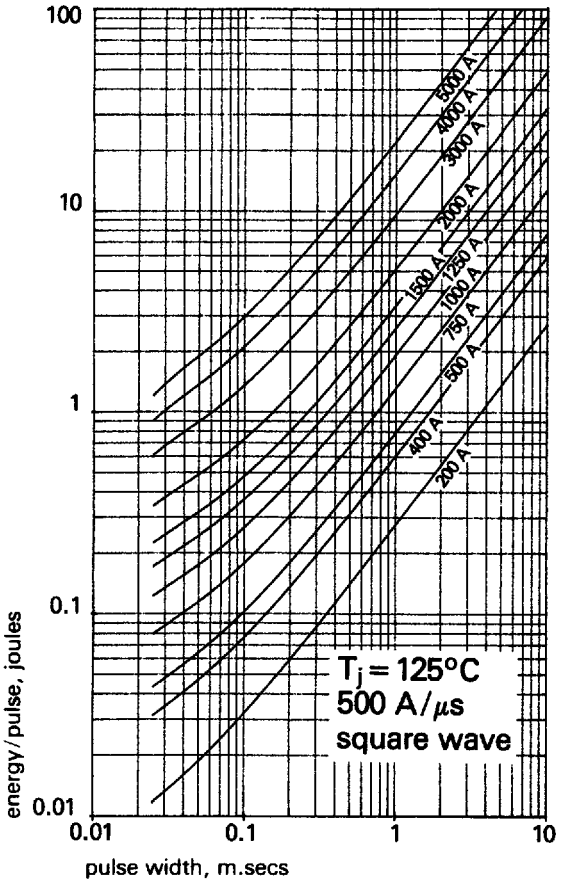


Figure 5 Energy/pulse v. pulse width

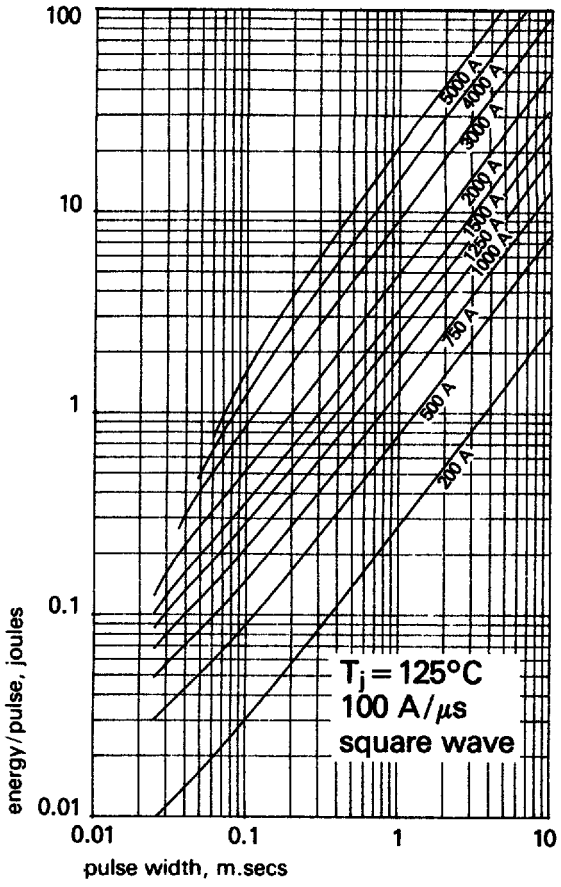


Figure 6 Energy/pulse v. pulse width

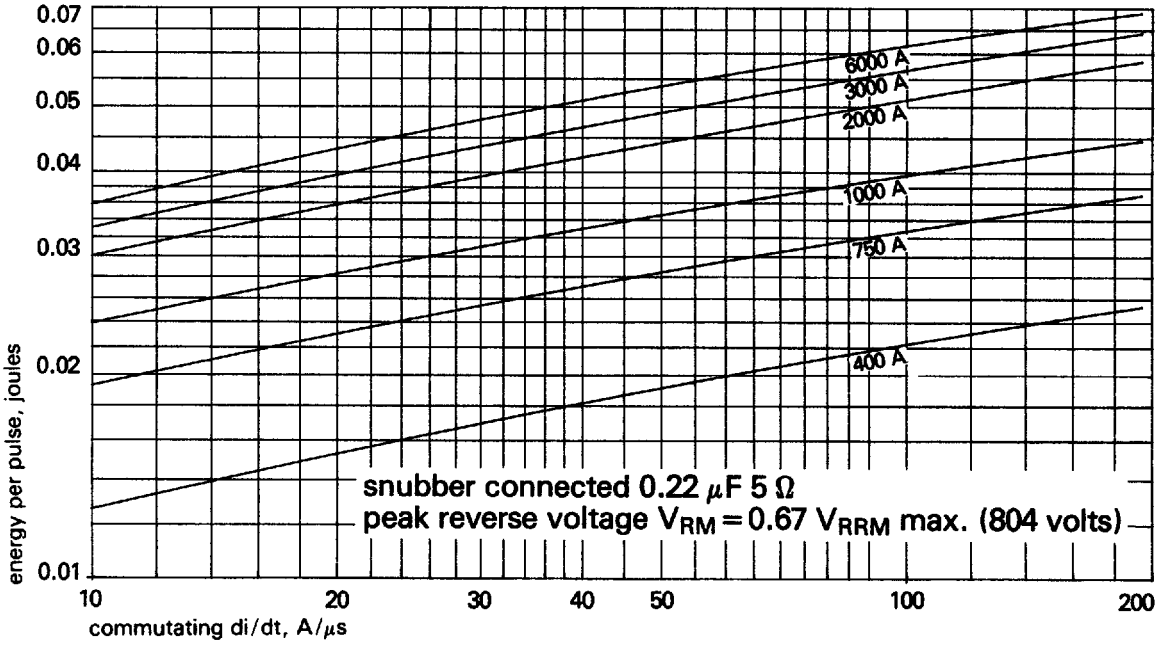


Figure 7 Max. reverse recovery energy loss per pulse at 125°C junction temperature and $V_{RM} = 804$ volts.

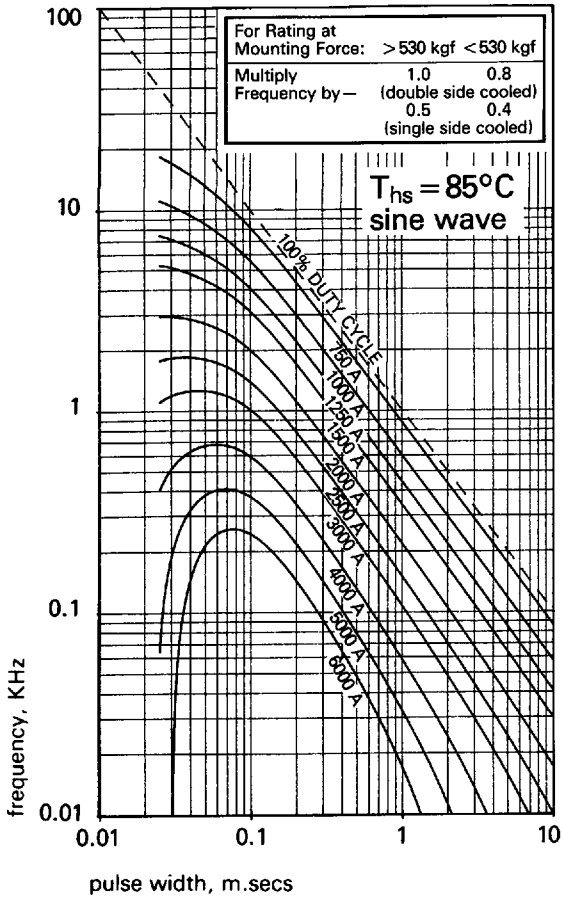


Figure 8 Frequency v. pulse width

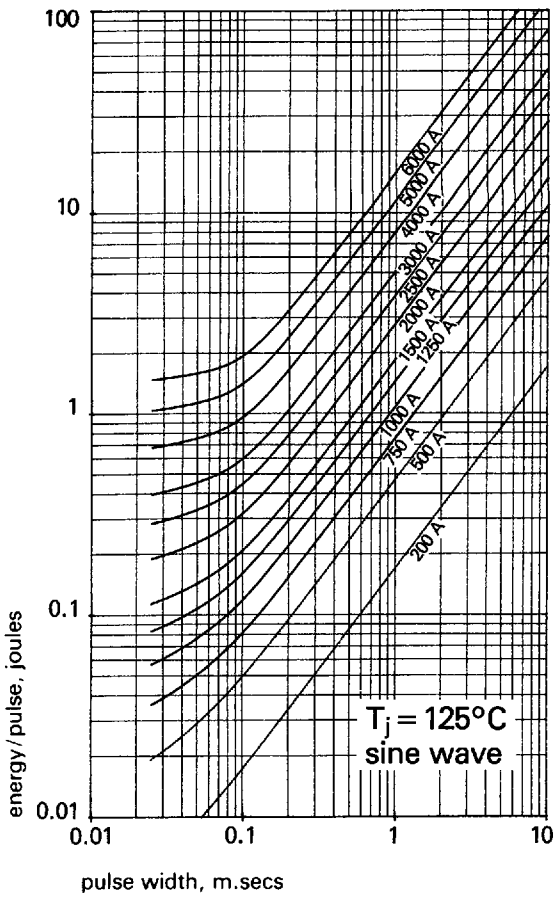


Figure 9 Energy/pulse v. pulse width

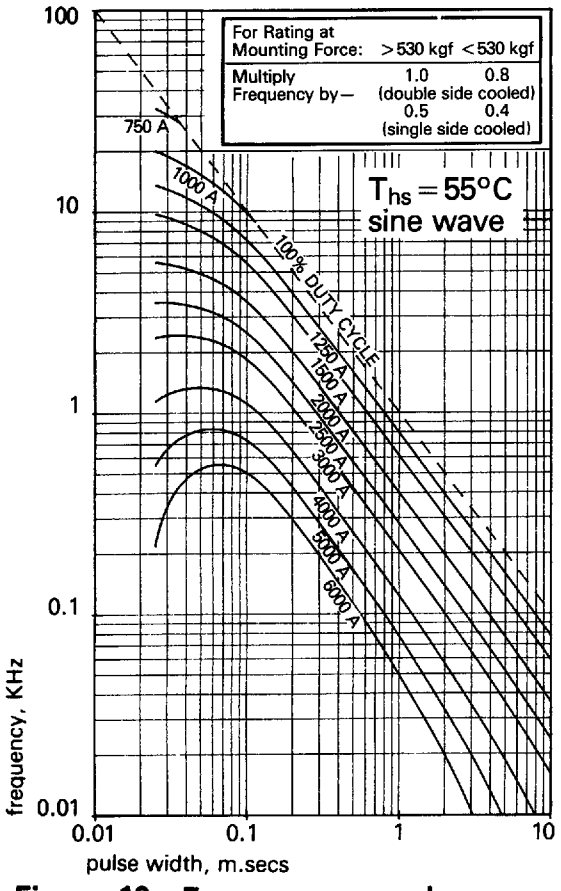


Figure 10 Frequency v. pulse width

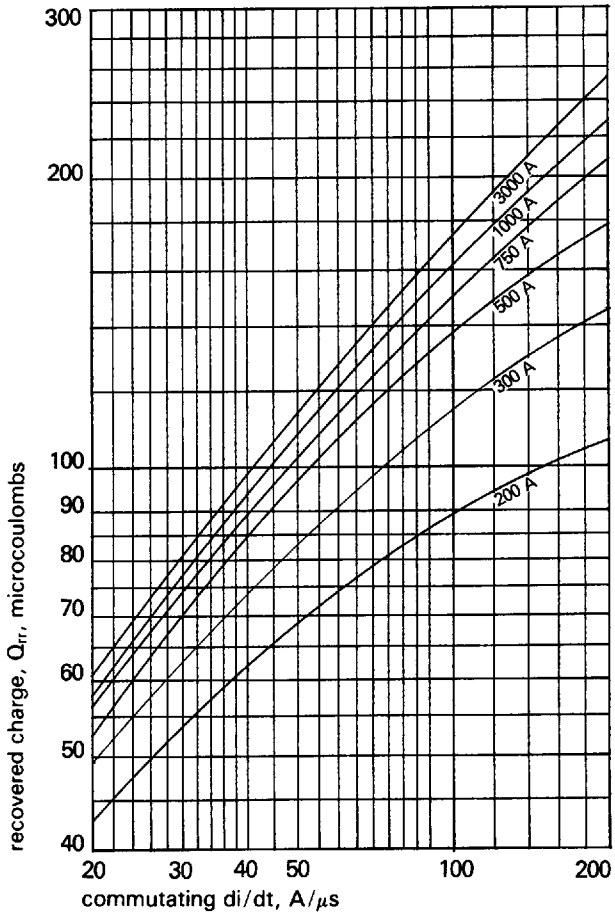


Figure 11 Maximum recovered charge at 125°C junction temperature

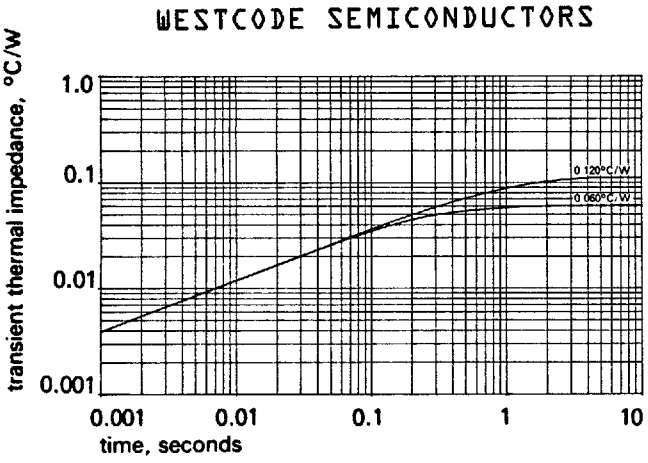


Figure 12 Junction to heatsink transient thermal impedance

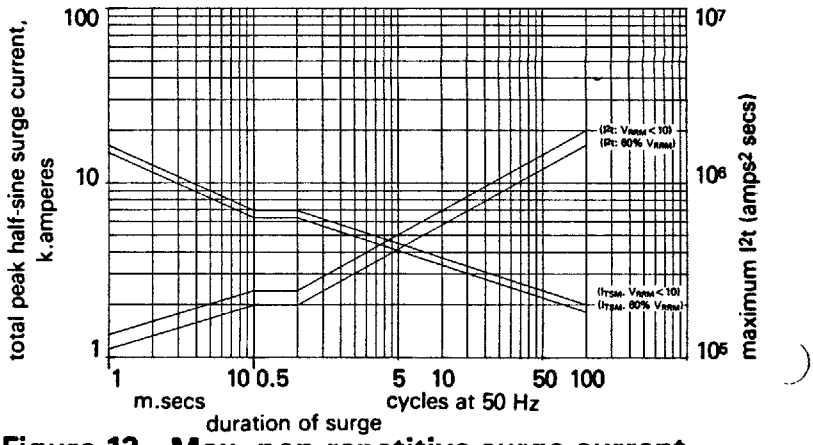


Figure 13 Max. non-repetitive surge current at initial junction temperature 125°C

gate may temporarily lose control of conduction angle

Note: This rating must not be interpreted as an intermittent rating

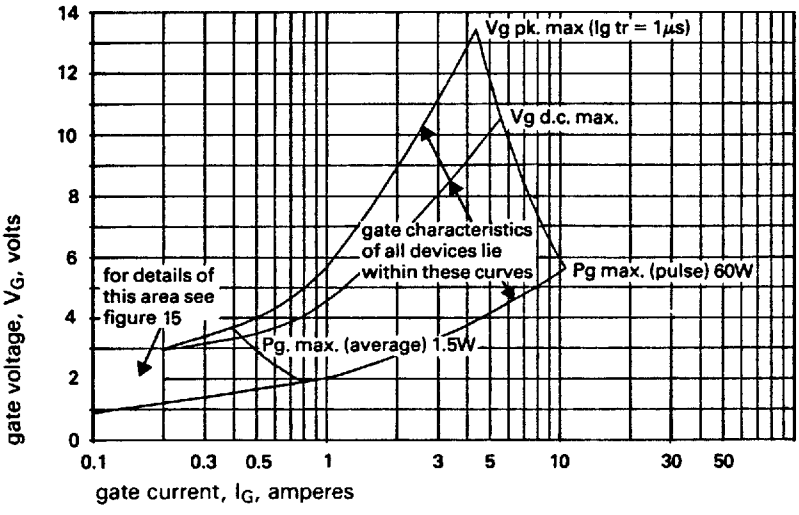


Figure 14 Gate characteristics at 25°C junction temperature

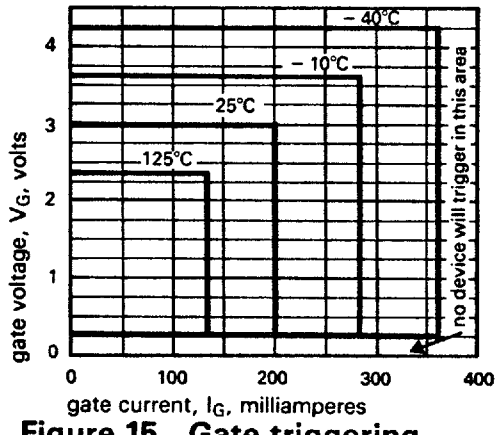


Figure 15 Gate triggering characteristics.

Trigger points of all thyristors lie within the areas shown Gate drive load line must lie outside appropriate I_G/V_G rectangle

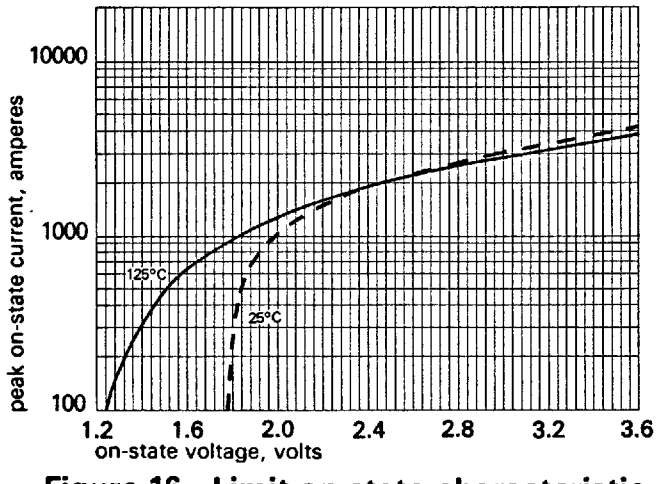
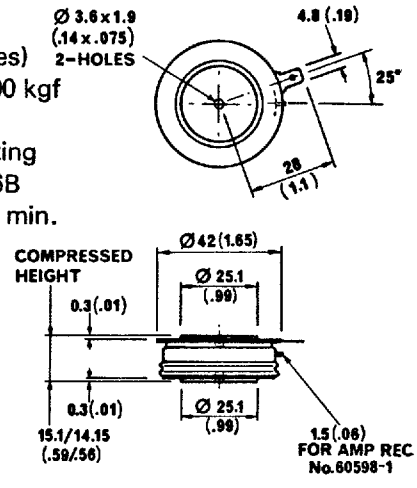


Figure 16 Limit on-state characteristic

dimensions in mm (inches)
Mounting force: 530-1000 kgf
Weight: 90 grams
Note: Box Clamp mounting
Box Clamp No. 101A226B
Mounting force: 365 kgf min.
$R_{th(j-hs)}$ 0.125°C/W



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In the interest of product improvement, Westcode reserves the right to change specifications at any time without notice.

WESTCODE SEMICONDUCTORS LTD

P.O. Box 57 Chippenham Wiltshire SN15 1JL England
Telephone Chippenham (0249) 654141 Telex 44751

HAWKER SIDDELEY
Westinghouse Brake and Signal Co. Ltd.

Printed by The Pheon Press, Bristol 2M585