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# CMOS 2K/4K-bit SERIAL E<sup>2</sup>PROM S-29255A/29355A

## ■ Instruction Set

Table 1

Instruction	Op code	Address		Data	
		S-29255A	S-29355A		
READ (Read data)	10101000	A <sub>0</sub> to A <sub>6</sub> 0	A <sub>0</sub> to A <sub>7</sub>	D <sub>0</sub> to D <sub>15</sub>	
PROGRAM (Program)	10100100	A <sub>0</sub> to A <sub>6</sub> 0	A <sub>0</sub> to A <sub>7</sub>	D <sub>0</sub> to D <sub>15</sub>	
WRAL (Write all)*	10100001	A <sub>0</sub> to A <sub>6</sub> 0	A <sub>0</sub> to A <sub>7</sub>	D <sub>0</sub> to D <sub>15</sub>	
ERAL (Erase all)*	10100010	xxxxxxx	xxxxxxx	—	
EWEN (Program enable)	10100011	xxxxxxx	xxxxxxx	—	
EWDS (Program disable)	10100000	xxxxxxx	xxxxxxx	—	
Status output	Busy flag	10101001	00xxxxxx	00xxxxxx	0 : BUSY 1 : READY
	Write permission		10xxxxxx	10xxxxxx	0 : Permission 1 : Inhibit
	ECC flag		01xxxxxx	01xxxxxx	"0" is always output**

x : Doesn't matter

\* : ERAL and WRAL are options. Normally these can not be used.

\*\* : S-29255A/29355A doesn't have redundant memory.

## ■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub>	V
Storage temperature under bias	T <sub>bias</sub>	-50 to +95	°C
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

## ■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Power supply voltage	V <sub>CC</sub>	Read	1.8	—	6.5	V	
		Write	2.7	—	6.5	V	
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 2.7 to 6.5V	$\overline{CS}$ , $5K$	0.8 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
			DI, RESET	0.7 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.7V		0.8 × V <sub>CC</sub>	—	V <sub>CC</sub>	V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 2.7 to 6.5V	$\overline{CS}$ , $5K$	0.0	—	0.2 × V <sub>CC</sub>	V
			DI, RESET	0.0	—	0.3 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.8 to 2.7V		0.0	—	0.2 × V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>		-40	—	+85	°C	

## ■ Rewriting Times

Table 4

(T<sub>a</sub> = -40°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rewriting times	N <sub>w</sub>	10 <sup>5</sup>	—	—	times/word

■ Pin Capacitance

Table 5

(Ta = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	—	—	8	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V	—	—	10	pF

■ DC Electrical Characteristics

Table 6

(Ta = -40°C to 85°C)

Parameter	Smb1	Conditions	Read/write operations						Read operation			Unit
			V <sub>CC</sub> = 5.0 V ± 10 %			V <sub>CC</sub> = 3.0 V ± 10 %			V <sub>CC</sub> = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I <sub>CC1</sub>	DO unloaded	—	—	2.0	—	—	1.0	—	—	0.5	mA
Current consumption (PROGRAM)	I <sub>CC2</sub>	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Table 7

(Ta = -40°C to 85°C)

Parameter	Smb1	Conditions	Read/write operations						Read operation			Unit
			V <sub>CC</sub> = 5.0 V ± 10 %			V <sub>CC</sub> = 2.7 to 6.5 V			V <sub>CC</sub> = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I <sub>SB</sub>	Input: V <sub>CC</sub> or GND	—	—	1.0	—	—	1.0	—	—	1.0	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V <sub>OL</sub>	CMOS I <sub>OL</sub> = 100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I <sub>OL</sub> = 2.1 mA	—	—	0.45	—	—	—	—	—	—	V
High level output voltage	V <sub>OH</sub>	CMOS V <sub>CC</sub> = 2.7 to 6.5 V: I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.3	—	—	V
		V <sub>CC</sub> = 1.8 to 2.7 V: I <sub>OH</sub> = -10 μA	—	—	—	—	—	—	—	—	—	V
		TTL I <sub>OH</sub> = -400 μA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V <sub>DH</sub>		1.5	—	—	1.5	—	—	1.5	—	—	V
Schmitt width	V <sub>WD</sub>	CS, SK	V <sub>CC</sub> ×0.1	—	—	V <sub>CC</sub> ×0.1	—	—	0.05	—	—	V

■ AC Electrical Characteristics

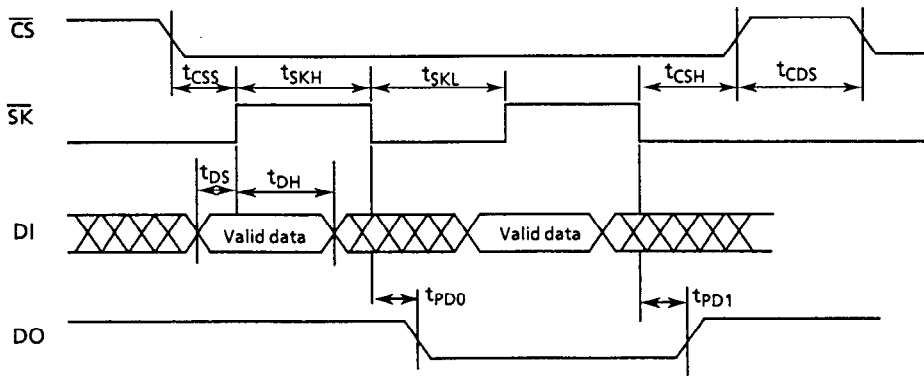
Table 8 Measuring conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100 pF

Table 9

( $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )

Parameter	Symbol	Read / Write operations						Read operation			Unit
		$V_{CC} = 5.0 \text{ V} \pm 10\%$			$V_{CC} = 2.7 \text{ to } 6.5 \text{ V}$			$V_{CC} = 1.8 \text{ to } 2.7 \text{ V}$			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{\text{CS}}$ setup time	$t_{\text{CSS}}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu\text{s}$
$\overline{\text{CS}}$ hold time	$t_{\text{CSH}}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu\text{s}$
$\overline{\text{CS}}$ setup time (CPU)	$t_{\text{CSS(CPU)}}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu\text{s}$
$\overline{\text{CS}}$ hold time (CPU)	$t_{\text{CSH(CPU)}}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu\text{s}$
$\overline{\text{CS}}$ deselect time	$t_{\text{CDS}}$	0.4	—	—	1.0	—	—	2.0	—	—	$\mu\text{s}$
Data setup time	$t_{\text{DS}}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu\text{s}$
Data hold time	$t_{\text{DH}}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu\text{s}$
1 data output delay	$t_{\text{PD1}}$	—	—	0.4	—	—	1.0	—	—	2.0	$\mu\text{s}$
0 data output delay	$t_{\text{PD0}}$	—	—	0.4	—	—	1.0	—	—	2.0	$\mu\text{s}$
Clock frequency	$f_{\text{SK}}$	0.0	—	2.0	0.0	—	1.0	0.0	—	0.2	MHz
Clock pulse width	$t_{\text{SKH}}, t_{\text{SKL}}$	0.25	—	—	0.5	—	—	2.5	—	—	$\mu\text{s}$
Output disable time	$t_{\text{HZ}}$	0	50	150	0	500	1000	—	—	—	ns
Program time	$t_{\text{PR}}$	—	4.0	10	—	4.0	10	—	—	—	ms



Input data is fetched at the rise of  $\overline{\text{SK}}$ .  
Output data is triggered at the fall of  $\overline{\text{SK}}$ .

Figure 3 Timing chart



Figure 4 Timing chart of  $t_{\text{CSS(CPU)}}$  and  $t_{\text{CSH(CPU)}}$  when connected to CPU

## ■ Operation

For each instruction, input op code, address and data per Table 1. After  $\overline{CS}$  goes from "H" to "L", DI is latched, synchronized with the rise of  $\overline{SK}$ . After the entire data is latched, the instructions input can be completed by changing  $\overline{CS}$  to "H". Even after changing  $\overline{CS}$  to low, instructions can not be latched by inputting a pulse to  $\overline{SK}$  while DI remains low.

NOTE: Between instructions,  $\overline{CS}$  must be "H" during  $t_{CDS}$ .

### 1. Read mode (READ)

The READ instruction reads data from the specified address.

Through the READ instruction, the op code and address are latched, synchronized with the rise of  $\overline{SK}$ . At the falling edge of the 16th  $\overline{SK}$  clock cycle from the start bit, (and all of the addresses are input), DO changes from high impedance (Hi-Z) status to data output status, and data is output, synchronized with the fall of  $\overline{SK}$ .

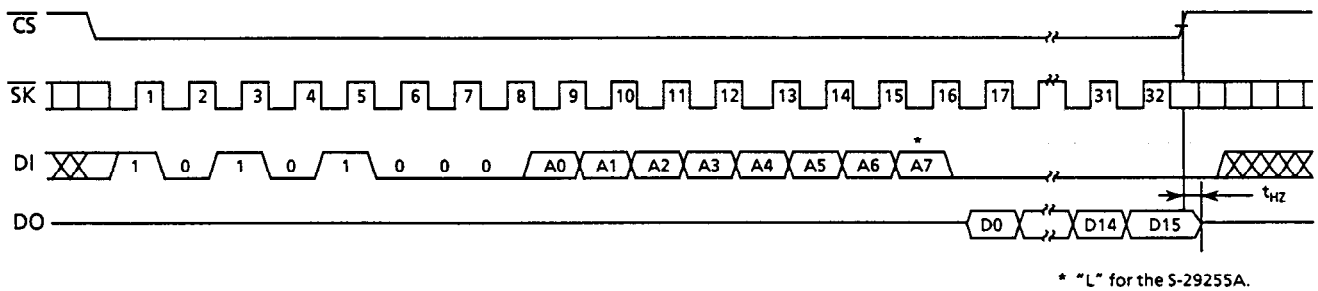


Figure 5

### 2. Write mode (PROGRAM, WRAL, and ERAL)

There are three write instructions, PROGRAM, WRAL, and ERAL. Each write instruction automatically starts the write operation to nonvolatile memory after completing the specified clock input. The write operation is completed in 10 ms ( $t_{PR}$  max.), and the average write period is 4 to 5 ms.

The S-29255A/29355A offer the following two methods to check the completion of the write operation to choose the shortest writing cycle.

- By reading the status of the  $RDY/\overline{BUSY}$  output pin  
While the write operation is continued, low level is output. And when the write operation is completed, high level is output.
- By reading the status output signal  
After inputting a write instruction, a status output instruction must be performed (for the status output instruction, refer to "4. Status output").

NOTE: ● After starting the write operation,  $\overline{CS}$  need not be "H".

- During the write operation, no instruction can be accepted except for status output. When using  $\overline{SK}$  or DI during the write operation, the  $\overline{SK}$  and DI signals should not be a status output instruction, or,  $\overline{CS}$  must be "H".
- The write operation can be performed when the RESET pin is at "L". After RESET is "H", even during write operation, the write operation is terminated, and data is unstable. Therefore, when writing is not performed, fix the RESET pin at "H" to inhibit all write operation and to avoid erroneous writing.
- When the status output instruction is input after the write instruction,  $\overline{CS}$  need not be "H".

# CMOS 2K/4K-bit SERIAL E<sup>2</sup>PROM S-29255A/29355A

## 2.1 Program (PROGRAM) mode

This mode writes 16-bit data to the specified address. After  $\overline{CS}$  goes to "L", input op code, address, and 16-bit data. The write operation starts at the rising edge of the 32nd  $\overline{SK}$  clock cycle from the start bit. It is not necessary to make the data be "1" before the data write operation.

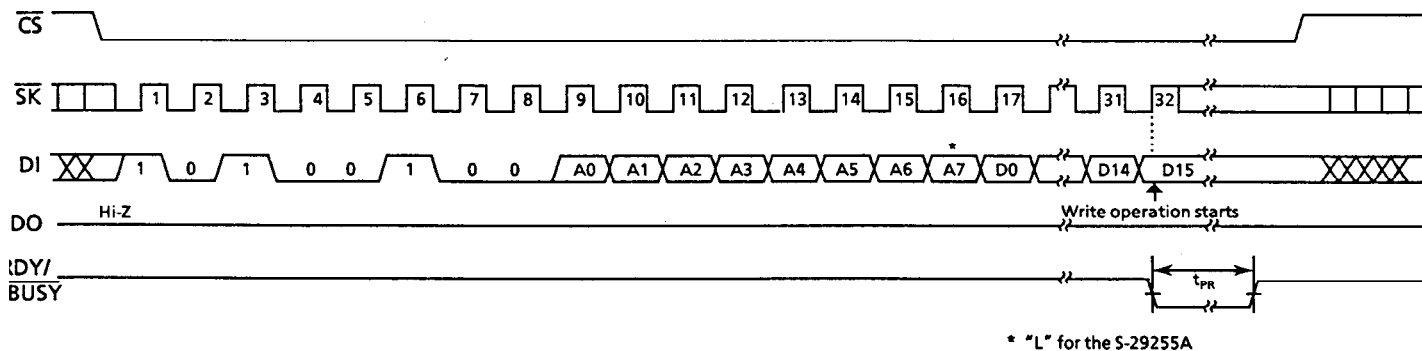


Figure 6

## 2.2 Write all (WRAL) mode: option

The same 16-bit data is written into all address areas in the memory. After  $\overline{CS}$  changes from "H" to "L", input the op code, address, and 16-bit data. The write operation starts at the rising edge of the 32nd  $\overline{SK}$  clock cycle from the start bit. It is not necessary to make the data be "1" before the data write operation.

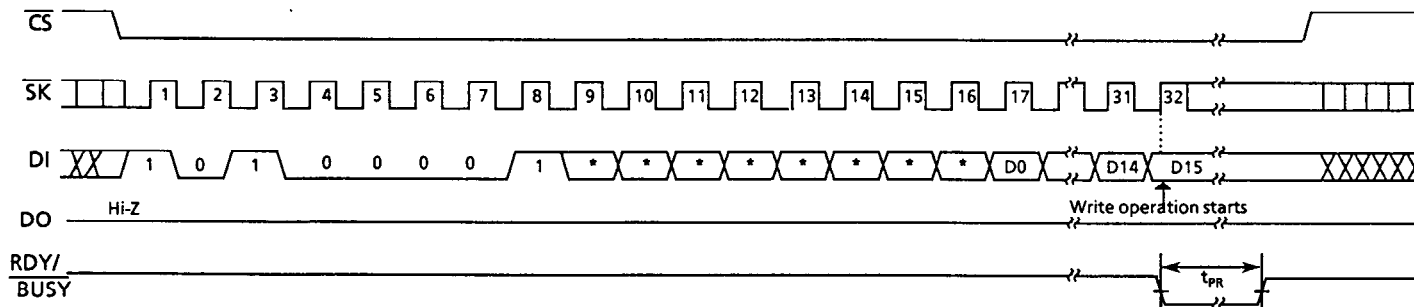


Figure 7

## 2.3 Erase all (ERAL) mode: option

Data in all address areas is erased. After erasing the data, all of the data is set to "1". After  $\overline{CS}$  changes from "H" to "L", input the op code and address. The erase operation starts at the rising edge of the 16th  $\overline{SK}$  clock cycle from the start bit.

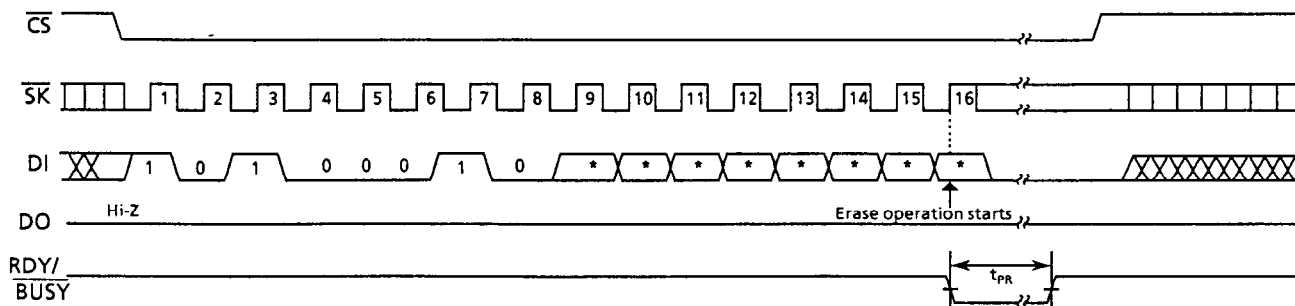


Figure 8

3. Program enable (EWEN) and program disable (EWDS) modes

EWEN enables the write operation, and EWDS disables the write operation. The status to enable the write operation is called the program enable mode, and the status to disable the write operation is called the program disable mode. The S-29255A/29355A is in program disable mode when the power is turned on. To prevent unexpected erroneous writing because of noise and CPU runaway, the S-29255A/29355A should be in program disable mode when writing is not performed.

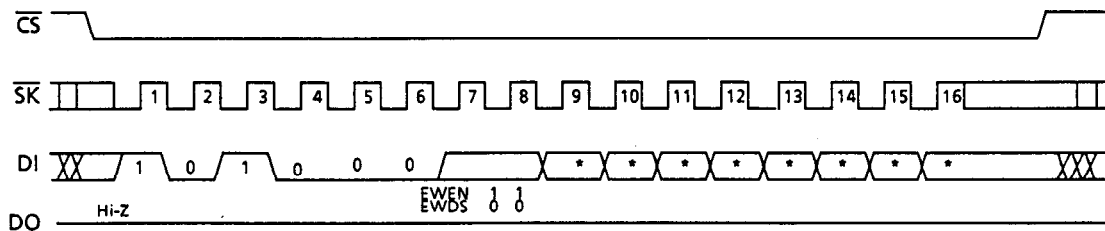


Figure 9

4. Status output

The status output instruction outputs several kinds of IC inside status (ready/busy, write inhibit/permit, and ECC set). Through the status output instruction, the op code and flag set code are latched, synchronized with the rise of  $\overline{SK}$ . At the falling edge of 16th clock cycle from the start bit, DO is changed from high impedance (Hi-Z) status to data output status, and the data that shows the IC inside status is output synchronized with the fall of  $\overline{SK}$ . The data is retained until  $\overline{CS}$  goes to "H".

NOTE : Even if the  $\overline{SK}$  and DI inputs are changed when outputting data, the output data is not changed.

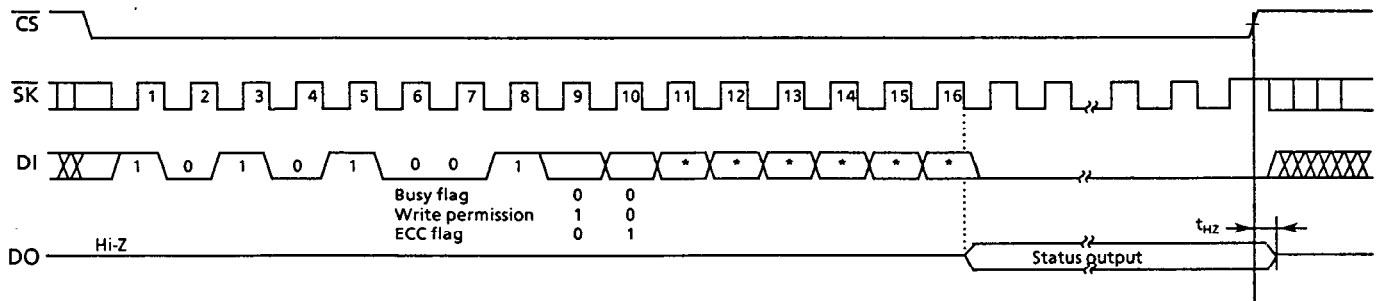


Figure 10

Table 10 IC inside status

Flag name	Flag set	"L" output	"H" output	Remarks
Write status flag	00	During writing	Completed writing	—
Write permission flag	10	Program enable mode	Program disable mode	—
ECC flag	01	Showing not modified	—	For maintaining compatibility with M6M80021/41, "L" is always output. Redundant memory is not included.

5. Reset operation

After RESET goes to "H" during the write operation, the write operation is terminated. At that time, only READ, EWEN, EWDS, and the status output instruction can be performed.

Although RESET can be connected with  $\overline{CS}$ , RESET must be fixed at "L" during writing. If RESET goes to "H" during writing, for 0.1 ms from the rise of RESET, no instruction except for status output can be accepted.



■ Three-wire Interface · DI-DO direct connecting

Although usually, a four-wire interface with  $\overline{CS}$ ,  $\overline{SK}$ , DI, and DO is used for configuring a serial interface, a three-wire interface can be also used for configuring a serial interface by connecting DI and DO. However, since the three-wire system has a possibility that the data output from the serial memory IC interferes with the data output from the CPU, install a resistor between DI and DO (See Figure 11) to give preference to data output from CPU into DI.

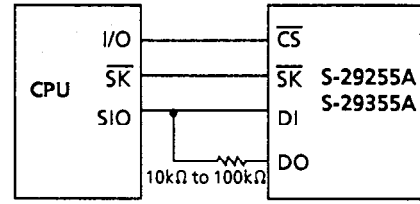


Figure 11

■ Dimensions (Unit:mm)

1. 8-pin DIP

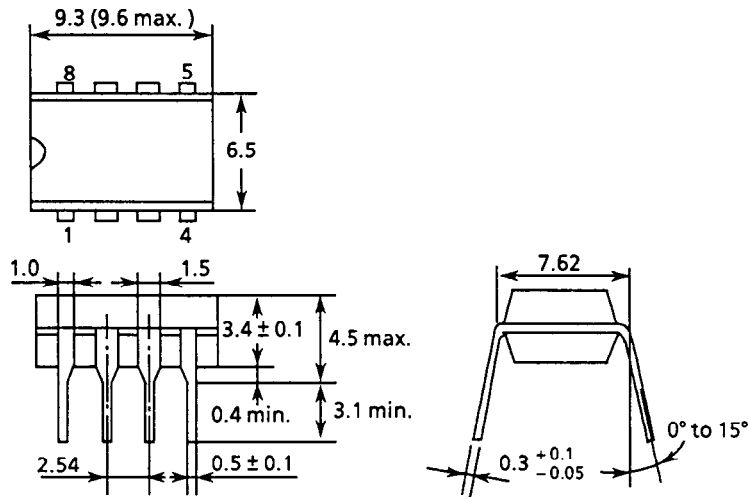


Figure 12

2. 8-pin SOP

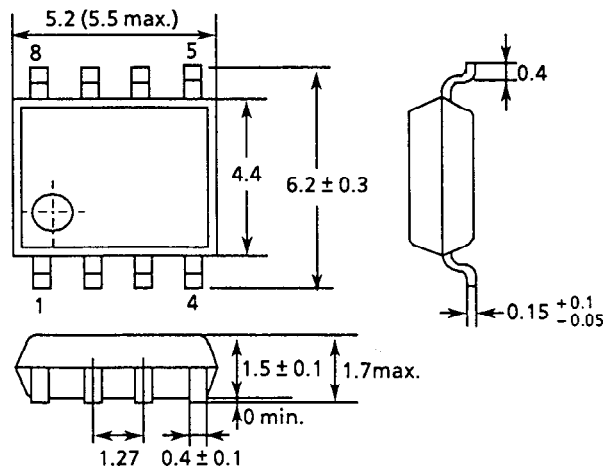
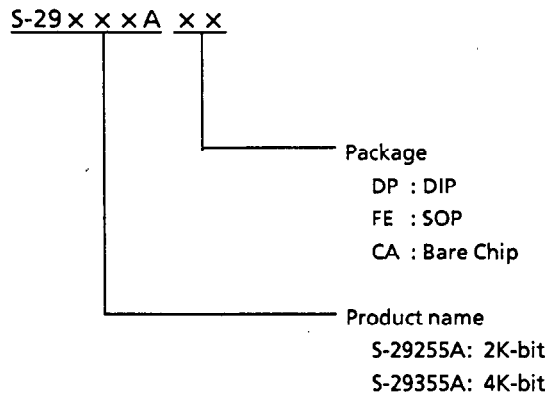


Figure 13

■ Ordering Information

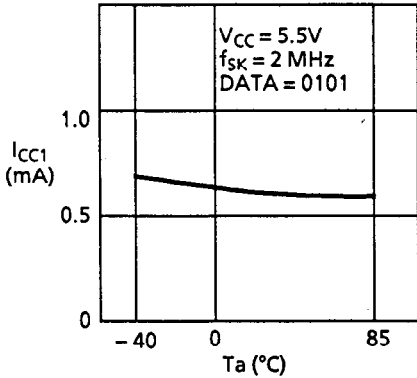


Note: Each bit is set to 1 before delivery (except bare chip) .

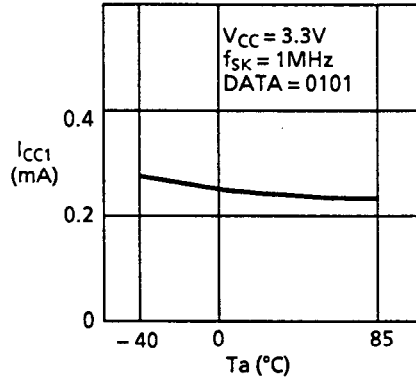
■ Characteristics

1. DC characteristics

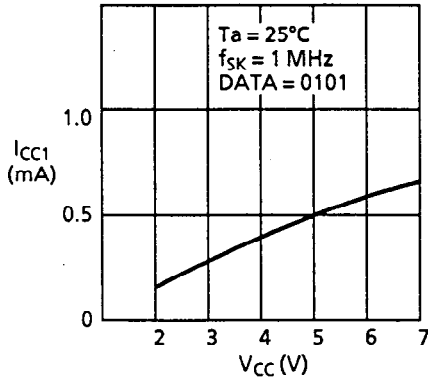
1.1 Current consumption (READ)  $I_{CC1}$  – Ambient temperature  $T_a$



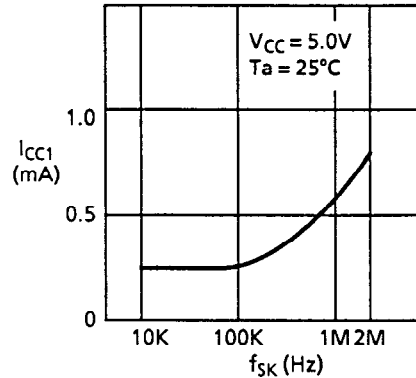
1.2 Current consumption (READ)  $I_{CC1}$  – Ambient temperature  $T_a$



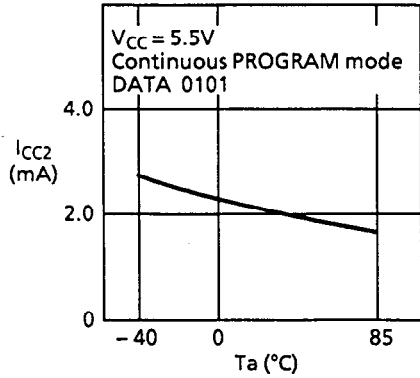
1.3 Current consumption (READ)  $I_{CC1}$  – Power supply voltage  $V_{CC}$



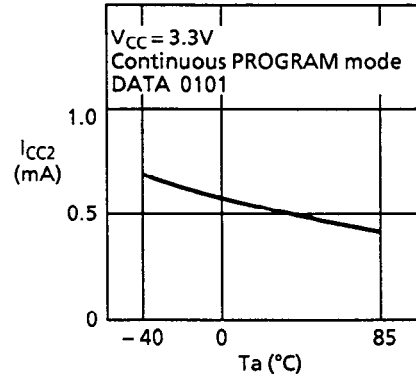
1.4 Current consumption (READ)  $I_{CC1}$  – Clock frequency  $f_{SK}$



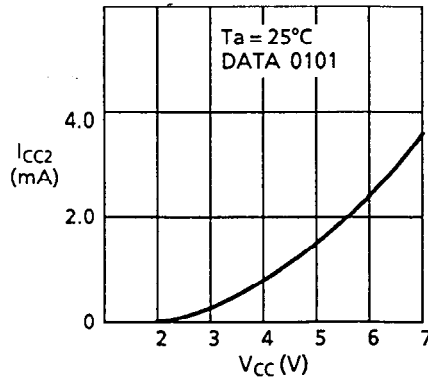
1.5 Current consumption (PROGRAM)  $I_{CC2}$  – Ambient temperature  $T_a$



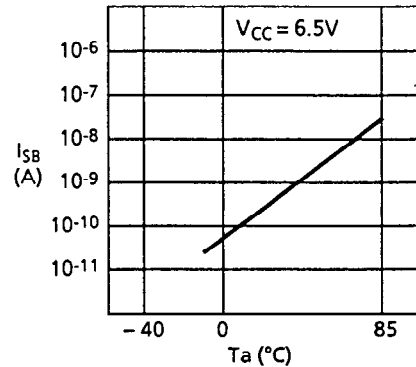
1.6 Current consumption (PROGRAM)  $I_{CC2}$  – Ambient temperature  $T_a$



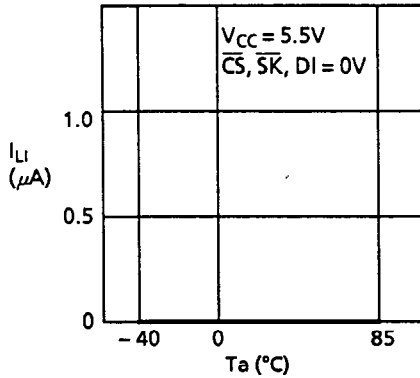
1.7 Current consumption (PROGRAM)  $I_{CC2}$  – Power supply voltage  $V_{CC}$



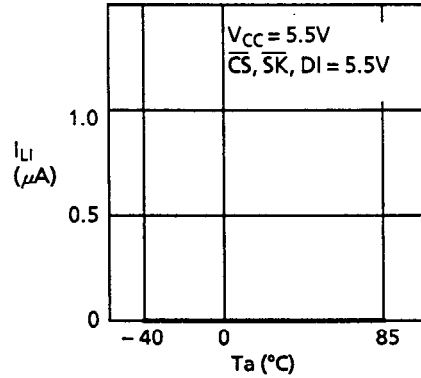
1.8 Standby current consumption  $I_{SB}$  – Ambient temperature  $T_a$



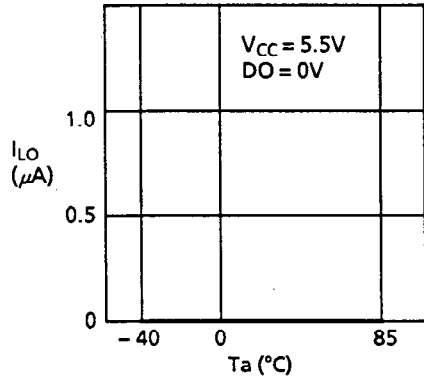
1.9 Input leakage current  $I_{LI}$  – Ambient temperature  $T_a$



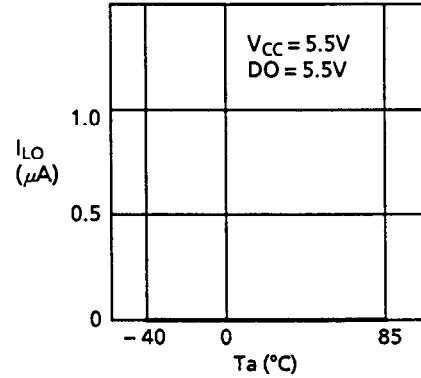
1.10 Input leakage current  $I_{LI}$  – Ambient temperature  $T_a$



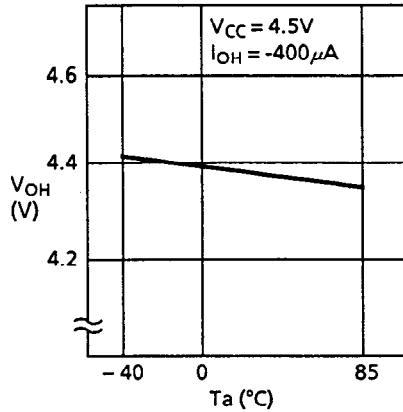
1.11 Output leakage current  $I_{LO}$  – Ambient temperature  $T_a$



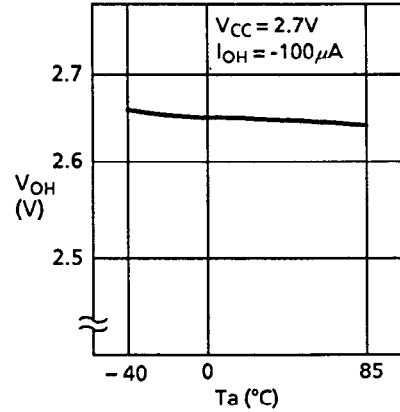
1.12 Output leakage current  $I_{LO}$  – Ambient temperature  $T_a$



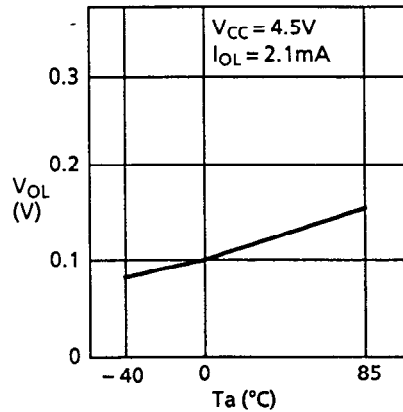
1.13 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



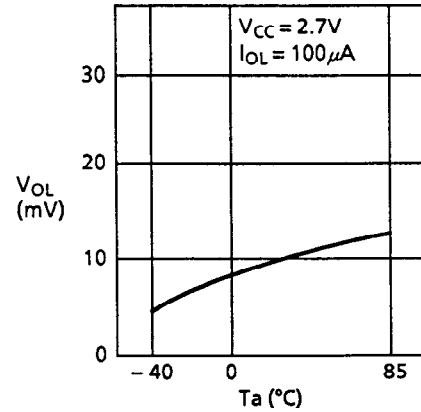
1.14 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



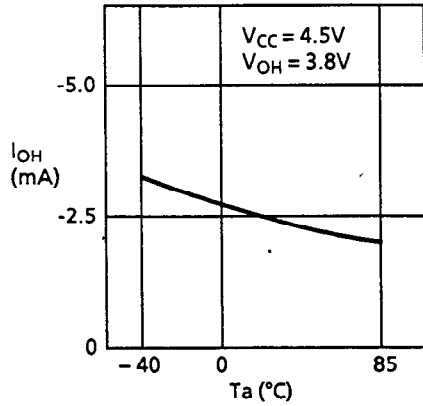
1.15 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



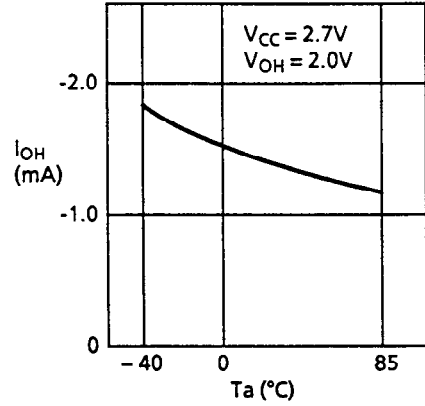
1.16 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



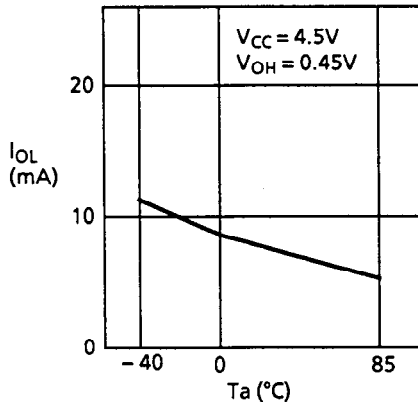
1.17 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



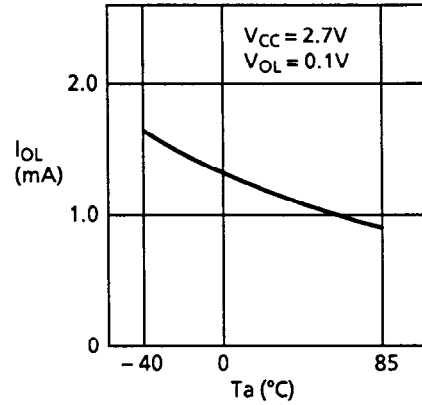
1.18 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



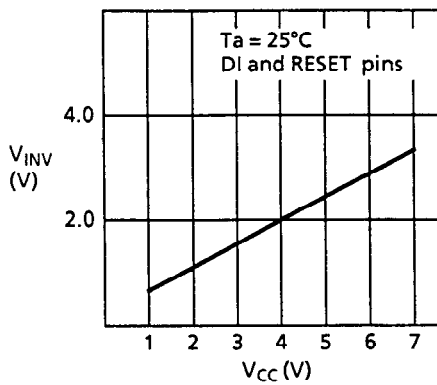
1.19 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



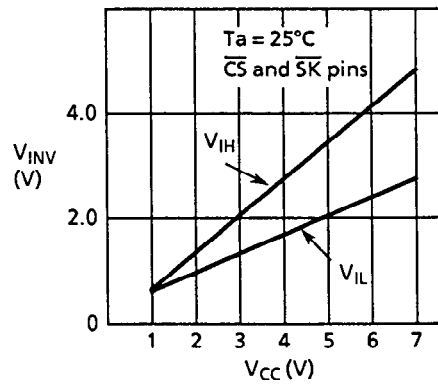
1.20 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



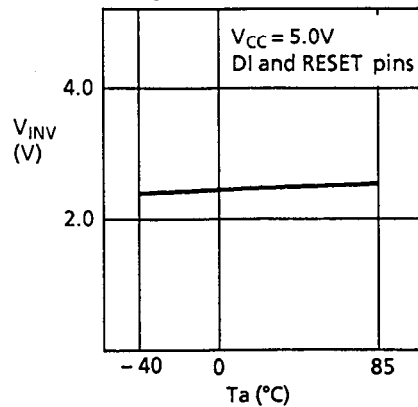
1.21 Input reversal voltage  $V_{INV}$  – Power supply voltage  $V_{CC}$



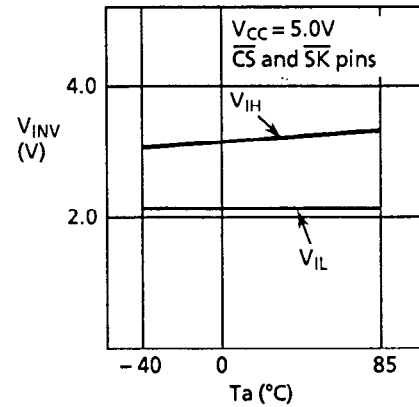
1.22 Input reversal voltage  $V_{INV}$  – Power supply voltage  $V_{CC}$



1.23 Input reversal voltage  $V_{INV}$  – Ambient temperature  $T_a$

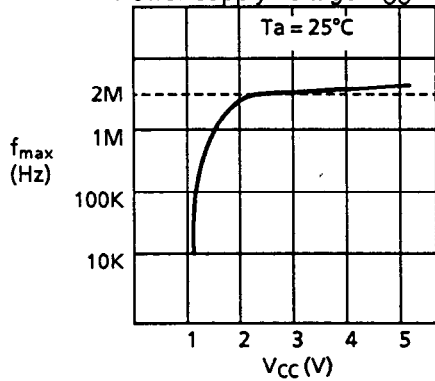


1.24 Input reversal voltage  $V_{INV}$  – Ambient temperature  $T_a$

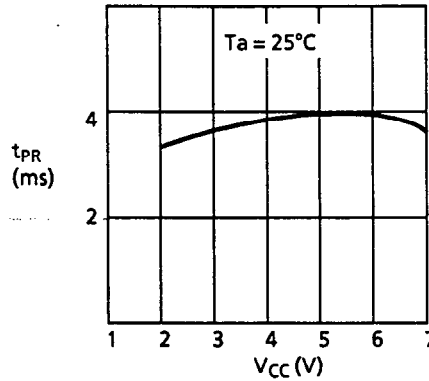


2. AC characteristics

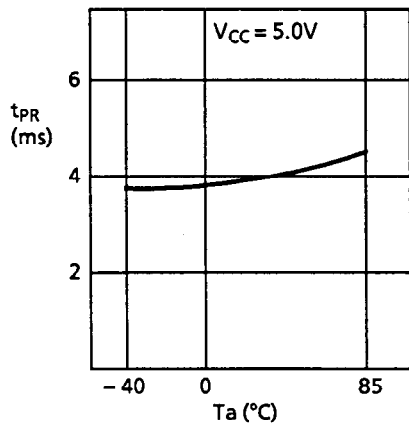
2.1 Maximum operating frequency  $f_{max}$  – Power supply voltage  $V_{CC}$



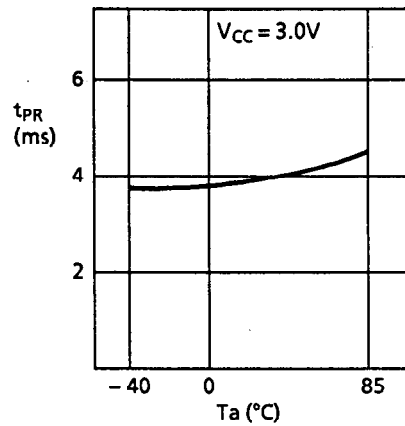
2.2 Program time  $t_{PR}$  – Power supply voltage  $V_{CC}$



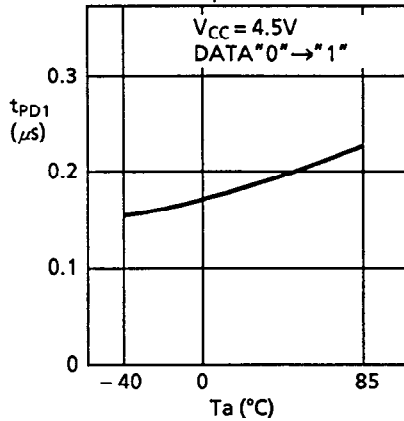
2.3 Program time  $t_{PR}$  – Ambient temperature  $T_a$



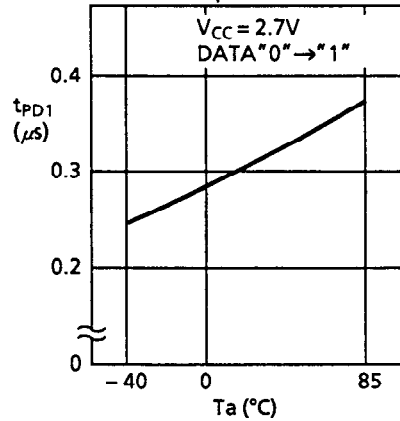
2.4 Program time  $t_{PR}$  – Ambient temperature  $T_a$



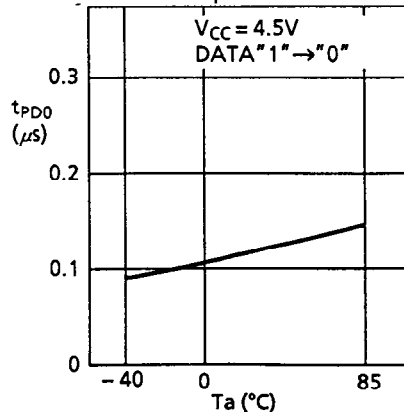
2.5.1 data output delay time  $t_{PD1}$  – Ambient temperature  $T_a$



2.6.1 data output delay time  $t_{PD1}$  – Ambient temperature  $T_a$



2.7.0 data output delay time  $t_{PD0}$  – Ambient temperature  $T_a$



2.8.0 data output delay time  $t_{PD0}$  – Ambient temperature  $T_a$

