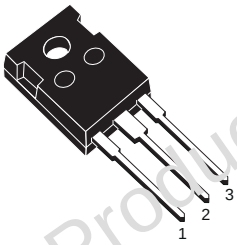
STW20NB50

N - CHANNEL 500V - 0.22Ω - 20A - TO-247
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW20NB50	500 V	< 0.25 Ω	20 A

- TYPICAL $R_{DS(on)}$ = 0.22 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ± 30V GATE TO SOURCE VOLTAGE RATING
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

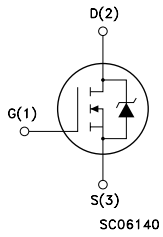


TO-247

DESCRIPTION

Using the latest high voltage technology, STMicroelectronics has designed an advanced family of power Mosfets with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS}(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (continuous) at T_c = 25 °C	20	A
I_D	Drain Current (continuous) at T_c = 100 °C	12.7	A
I_{DM}(•)	Drain Current (pulsed)	80	A
P_{tot}	Total Dissipation at T_c = 25 °C	250	W
	Derating Factor	2	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 20A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ T_{JMAX}

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.5	$^oC/W$
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	30	oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.1	$^oC/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	^oC

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	20	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\ ^oC$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	1000	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\ ^oC$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating $T_c = 125\ ^oC$			10 100	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$ V $I_D = 10$ A		0.22	0.25	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	20			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 10$ A	9	13.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$		3600 460 55	4700 600 75	pF pF pF

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ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 250 V I_D = 10 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		32 15	43 21	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V I_D = 20 A V_{GS} = 10 V		85 21 37	110	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400 V I_D = 20 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		20 25 17	27 33 62	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 20 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		700 9 25		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

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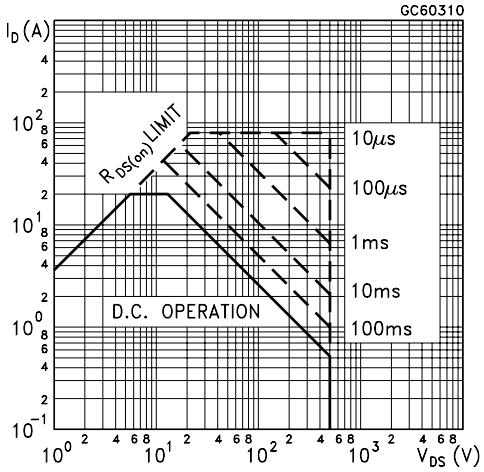
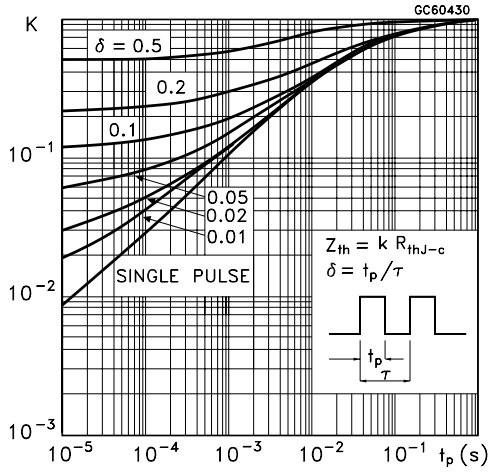
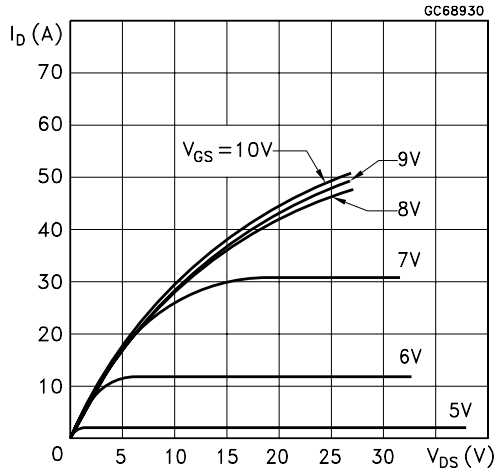
Safe Operating Area



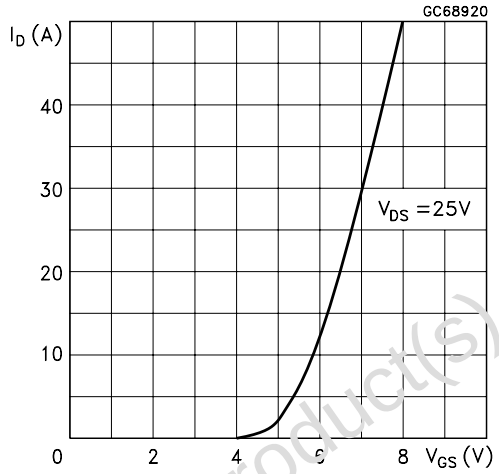
Thermal Impedance



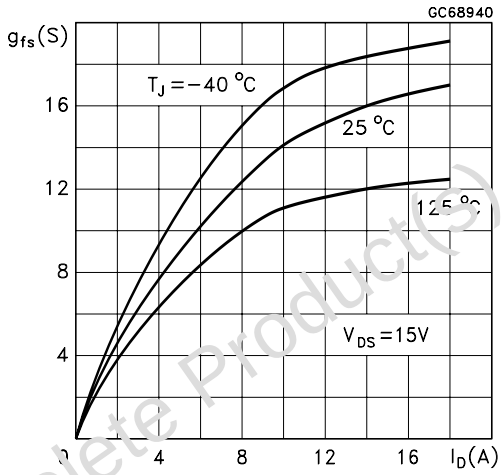
Output Characteristics



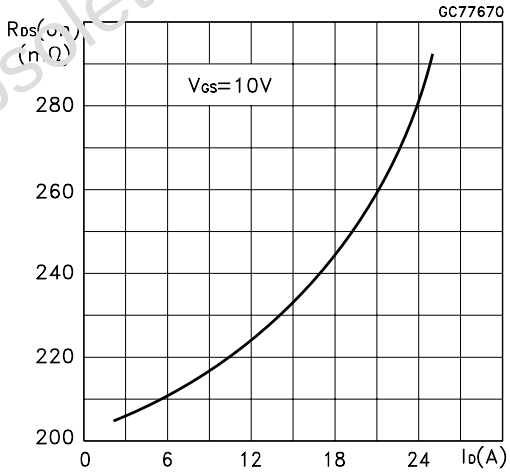
Transfer Characteristics



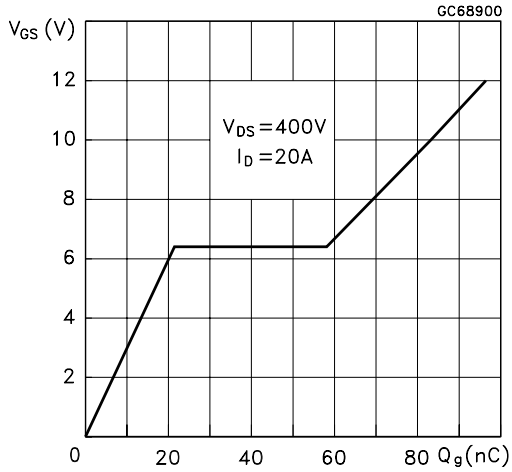
Transconductance



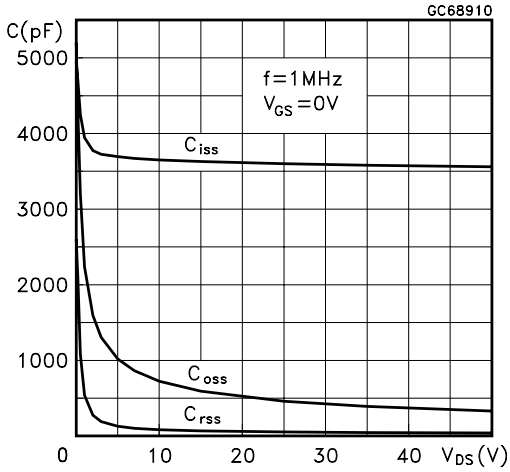
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage



Capacitance Variations



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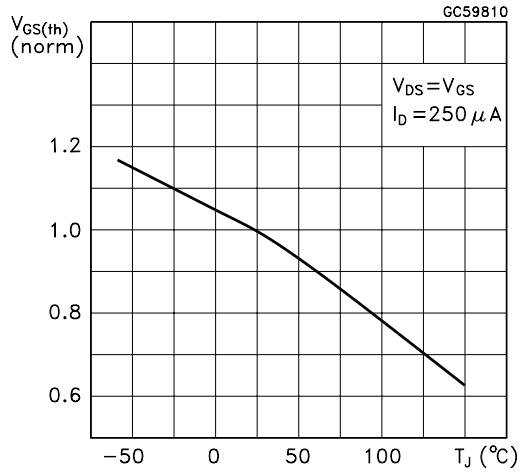
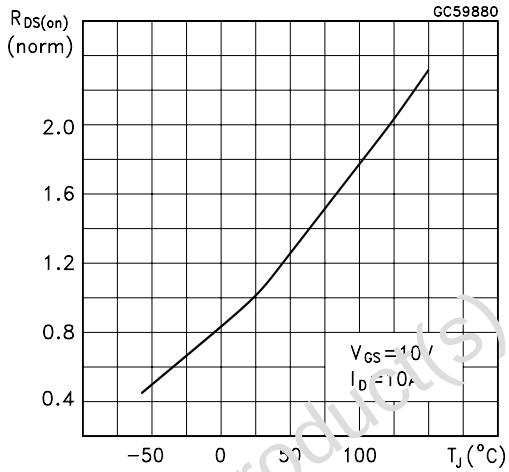
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

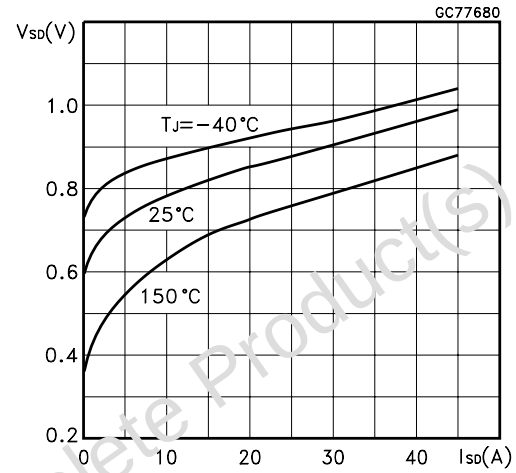


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Fig. 1: Unclamped Inductive Load Test Circuit

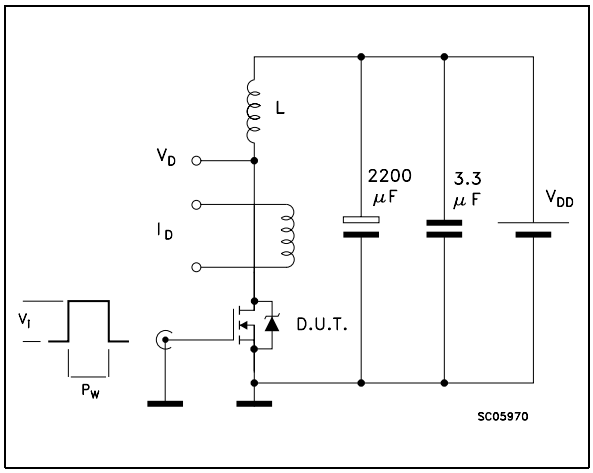


Fig. 2: Unclamped Inductive Waveform

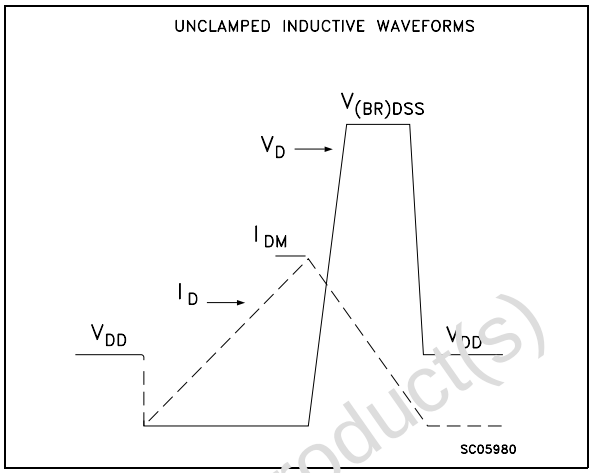


Fig. 3: Switching Times Test Circuits For Resistive Load

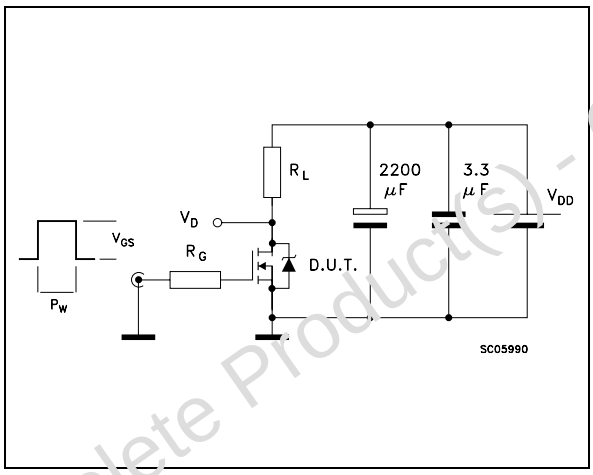


Fig. 4: Gate Charge test Circuit

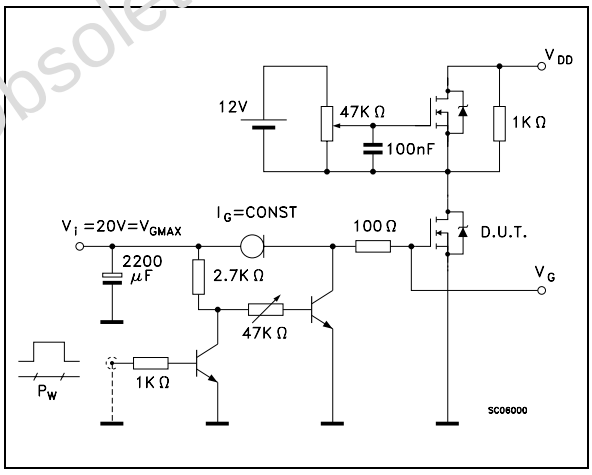
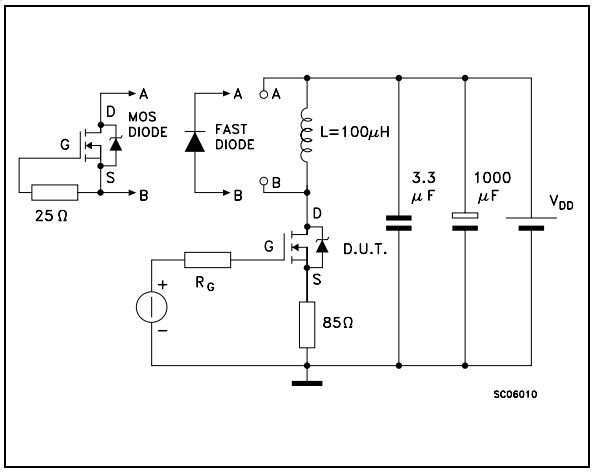


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



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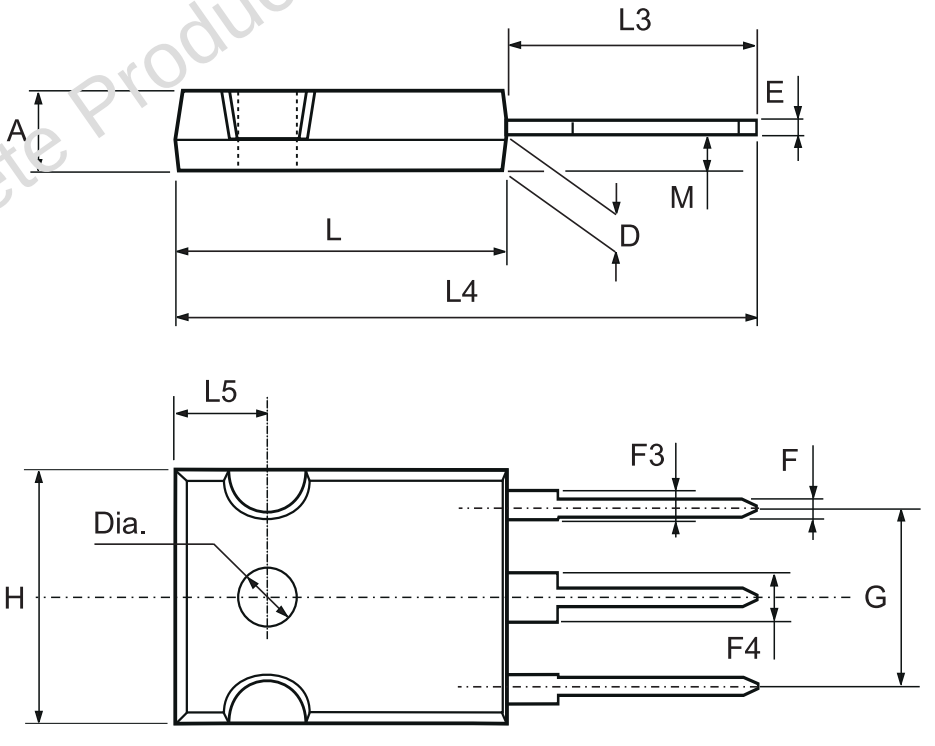
TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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