Brushless DC motor drive circuit | TDA5140A

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.8 A output current (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- VCR
- Laser beam printer
- Fax machine
- Blower
- Automotive

GENERAL DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	$I_O = 100$ mA	–	0.93	1.05	V
I_{LIM}	current limiting	$V_{VMOT} = 10$ V; $R_O = 3.9\ \Omega$	0.7	0.8	1	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs $I_O = 0$ mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5140A	18	DIL	plastic	SOT102
TDA5140AT	20	SOL	plastic	SOT163A

Brushless DC motor drive circuit TDA5140A

BLOCK DIAGRAM

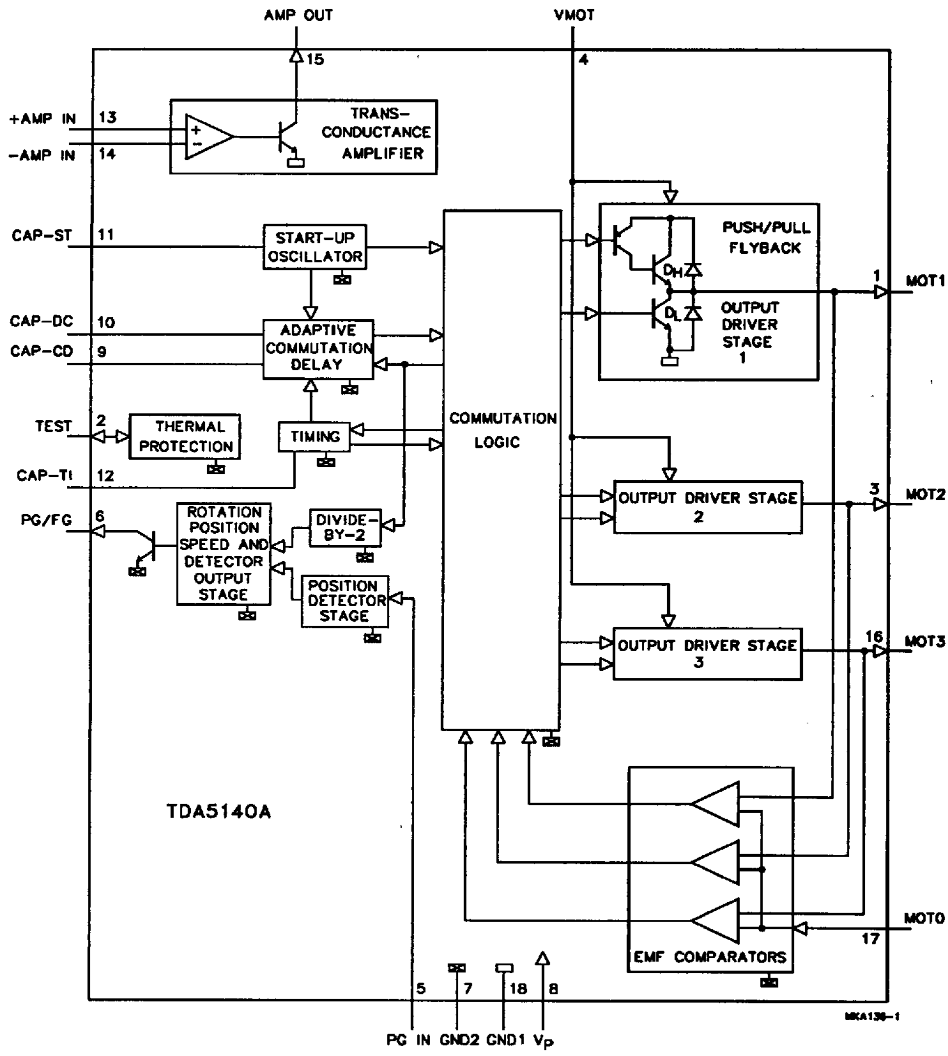

Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	DESCRIPTION
MOT1	1	1	driver output 1
TEST	2	2	test input/output
n.c.		3	not connected
MOT2	3	4	driver output 2
VMOT	4	5	input voltage for the output driver stages
PG IN	5	6	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	ground supply return for control circuits
V_P	8	9	positive supply voltage
CAP-CD	9	10	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	external capacitor connection for start-up oscillator
CAP-TI	12	13	external capacitor connection for timing
+AMP IN	13	14	non-inverting input of the transconductance amplifier
–AMP IN	14	15	inverting input of the transconductance amplifier
AMP OUT	15	16	transconductance amplifier output (open collector)
MOT3	16	17	driver output 3
n.c.	–	18	not connected
MOT0	17	19	input from the star point of the motor coils
GND1	18	20	ground (0 V) motor supply return for output stages

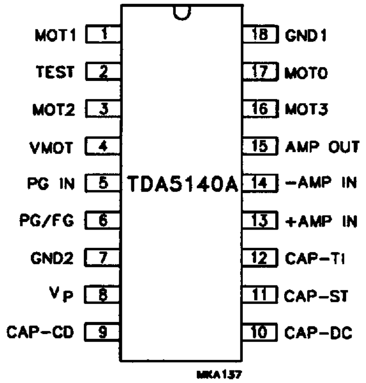

Fig.2 Pin configuration (SOT102; DIL18).

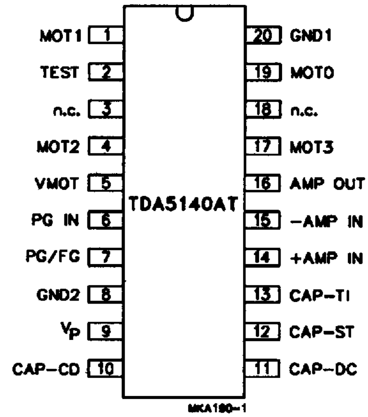

Fig.3 Pin configuration (SOT163A; SO20L).

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (0.8 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Accurate frequency generator (FG) by using the motor EMF.
- Amplifier for external position generator (PG) signal.
- Suitable for use with a wide tolerance, external PG sensor.
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		−0.5	17	V
V_O	output voltage				
	AMP OUT and PG/FG		GND	V_P	V
	MOT1, MOT2 and MOT3		−1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Figs 4 and 5	–	–	W
V_{es}	electrostatic handling	see "Handling"	–	500	V

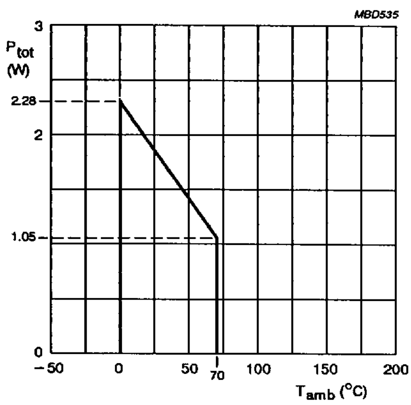

Fig.4 Power derating curve (SOT102; DIL18).

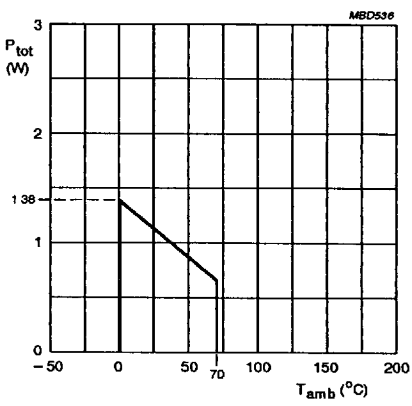

Fig.5 Power derating curve (SOT163A; SO20L).

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C class 2"*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

Brushless DC motor drive circuit TDA5140A

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0; centre tap						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV
MOT1, MOT2 and MOT3						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
		I_O = 500 mA	–	1.65	1.80	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 6.8 Ω	0.7	0.8	1	A
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AMP OUT (open collector)						
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		–0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		–0.3	–	+5	V
I_b	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_{hys}	comparator input hysteresis		–	±8	–	mV
PG/FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	18	µs
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	µA
I_{source}	output source current		–2.5	–2.0	–1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	µA
I_{source}	output source current	0.05 V < V_{CAP-TI} < 0.3 V	–	–57	–	µA
		0.3 V < V_{CAP-TI} < 2.2 V	–	–5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

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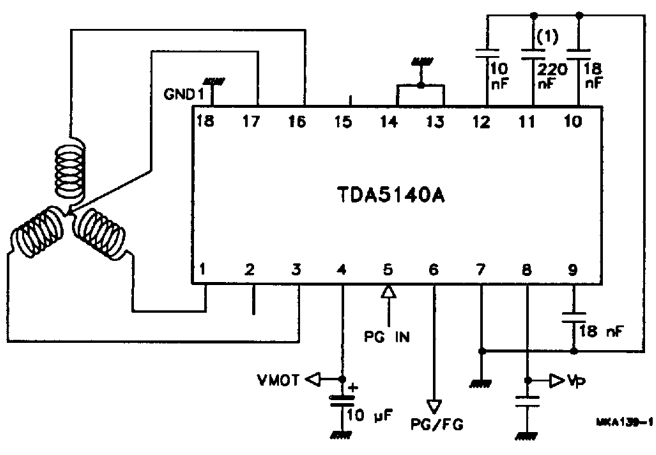
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	μA
I_{source}	output source current		−5.3	−8.1	−11	μA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	μA
I_{source}	output source current		−20.9	−15.5	−10.1	μA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.6 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.7)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

Table 1 Output states.

STATE	MOT1(1)	MOT2(1)	MOT3(1)
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high impedance OFF-state.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The detected zero-crossings are used to provide speed information. The information has been made available on the PG/FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140A also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140A is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

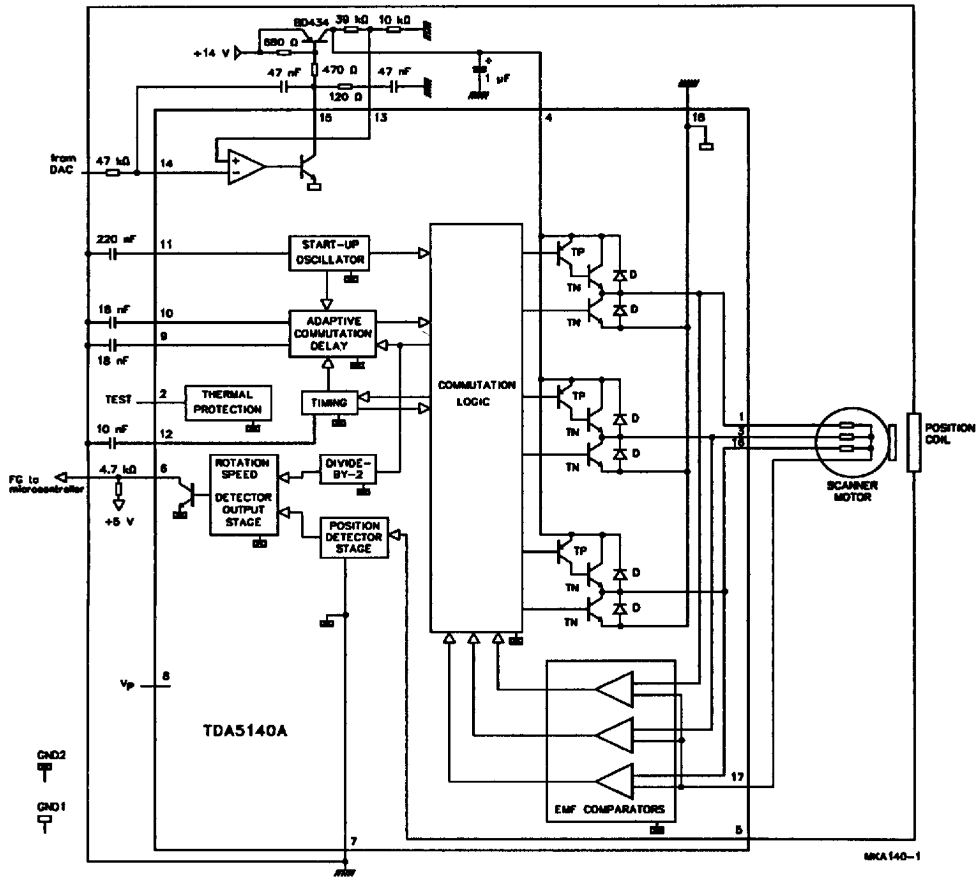


Fig.7 Typical application of the TDA5140A as a scanner driver, with use of OTA.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 × C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140A will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J (kg.m^2)

Example: J = 72 × 10^{-6} kg.m^2, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{c1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 × C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 8 illustrates typical voltage waveforms.

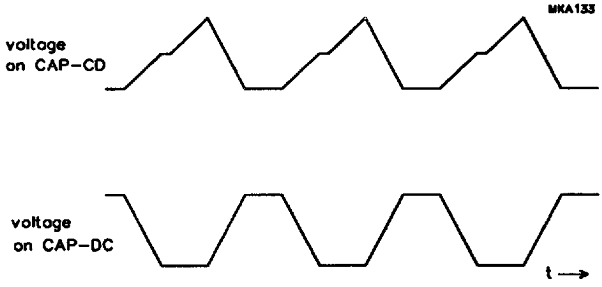


Fig.8 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

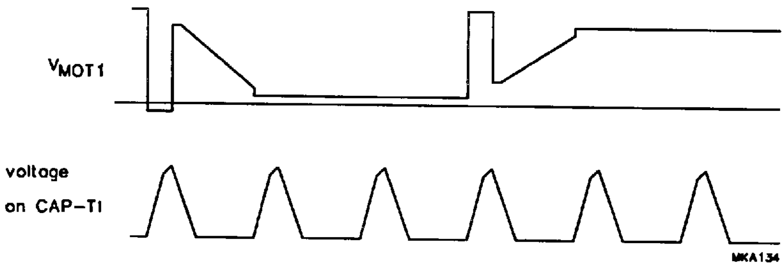
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.9.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.9 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5140A by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A 3-phase motor with 6 magnetic pole-pairs at 1 500 rpm and with a full-wave drive has a commutation frequency of $25 \times 6 \times 6 = 900$ Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 18 μs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.10).

For more information also see *"application note EIE/AN 93014"*.

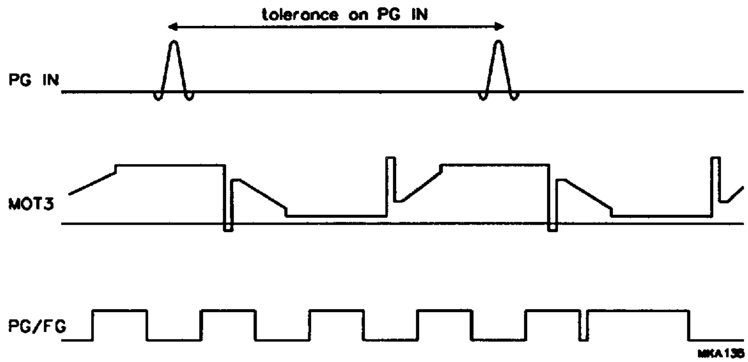


Fig.10 Timing and the FG and PG IN signals.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive-going voltage (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.10).

The voltage requirements of the PG IN input are such that an inexpensive pick-up coil can be used as a sensor (see Fig.11).

Example: If p = 6, then one revolution contains 6 × 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

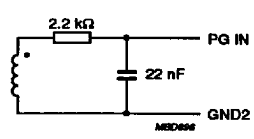


Fig.11 Pick-up coil as PG sensor.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to $V_P - 1.7$ V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (−AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.7).

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking, the motor voltage (via the flyback diodes and the impedance on VMOT) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.