TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (Ultra-High-Speed U-MOSIII)

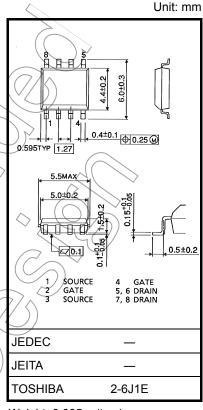
# **TPC8214-H**

High-Efficiency DC / DC Converter Applications CCFL Inverters

- · Small footprint due to a small and thin package
- · High-speed switching
- Small gate charge: Q<sub>SW</sub> = 2.0 nC (typ.)
- Low drain-source ON-resistance:  $R_{DS}(ON) = 130 \text{ m}\Omega$  (typ.)
- High forward transfer admittance: |Y<sub>fS</sub>| =5.4 S (typ.)
- Low leakage current:  $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 100 \text{ V)}$
- Enhancement mode:  $V_{th}$  = 1.1 to 2.3 V ( $V_{DS}$  = 10 V,  $I_D$  = 1 mA)

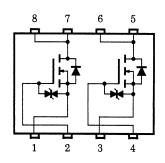
### Absolute Maximum Ratings (Ta = 25°C)

Cha	racteristic	Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	100	٧
Drain-gate volta	ge (R <sub>GS</sub> = 20 kΩ)	$V_{DGR}$	100	V
Gate-source vol	tage	V <sub>GSS</sub> 〈	±20,	/y
Drain current	D C (Note 1)	ID (	2.2	
Drain current	Pulse (Note 1)	IDP (	8.8	A
Drain power dissipation	Single-device operation (Note 3a)	PD(1)	1.5	
(t = 10 s) (Note 2a)	Single-device value at dual operation (Note 3b)	P <sub>D</sub> (2)	1.1	<b>W</b>
Drain power	Single-device operation (Note 3a)	PD (1)	0.75	$\rightarrow$
dissipation (t = 10 s) (Note 2b)	Single-device value at dual operation (Note 3b)	P <sub>D 2)</sub>	0.45	W
Single-pulse avalanche energy (Note 4)		E <sub>AS</sub>	3.9	mJ
Avalanche currer	nt	IAR	2.2	Α
Repetitive avalar (Note	nche energy e 2a, Note 3b, Note 5)	EAR	0.026	mJ
Channel tempera	ature	Tch	150	°C
Storage tempera	ture range	Tstg	-55~150	°C



Weight: 0.085 g (typ.)

### **Circuit Configuration**



Note: For Notes 1 to 5, refer to the next page.

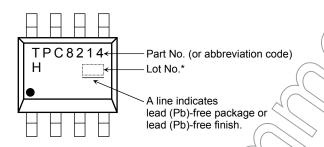
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

#### **Thermal Characteristics**

Characteristic	Symbol	Max	Unit	
Thermal registeres, channel to ambier	Single-device operation (Note 3a)	R <sub>th (ch-a) (1)</sub>	83.3	
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	Single-device value at dual operation (Note 3b)	R <sub>th (ch-a) (2)</sub>	114	°C/W
Thermal resistance, shapped to embient	Single-device operation (Note 3a)	R <sub>th (ch-a) (1)</sub>	167	
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	Single-device value at dual operation (Note 3b)	R <sub>th</sub> (ch-a) (2)	278	

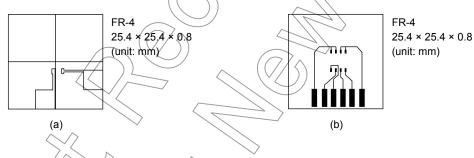
### Marking



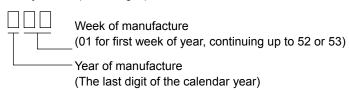
Note 1: The channel temperature should not exceed 150°C during use.

#### Note 2:

- a) Device mounted on a glass-epoxy board (a)
- b) Device mounted on a glass-epoxy board (b)



- Note 3:
  - a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)
- b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)
- Note 4:  $V_{DD}$  = 50 V,  $T_{ch}$  = 25°C (Initial), L = 1.0 mH,  $R_G$  = 25  $\Omega$ ,  $I_{AR}$  = 2.2 A
- Note 5: Repetitive rating: pulse width limited by maximum channel temperature
- Note 6: on the lower left of the marking indicates Pin 1.
  - \* Weekly code: (Three digits)



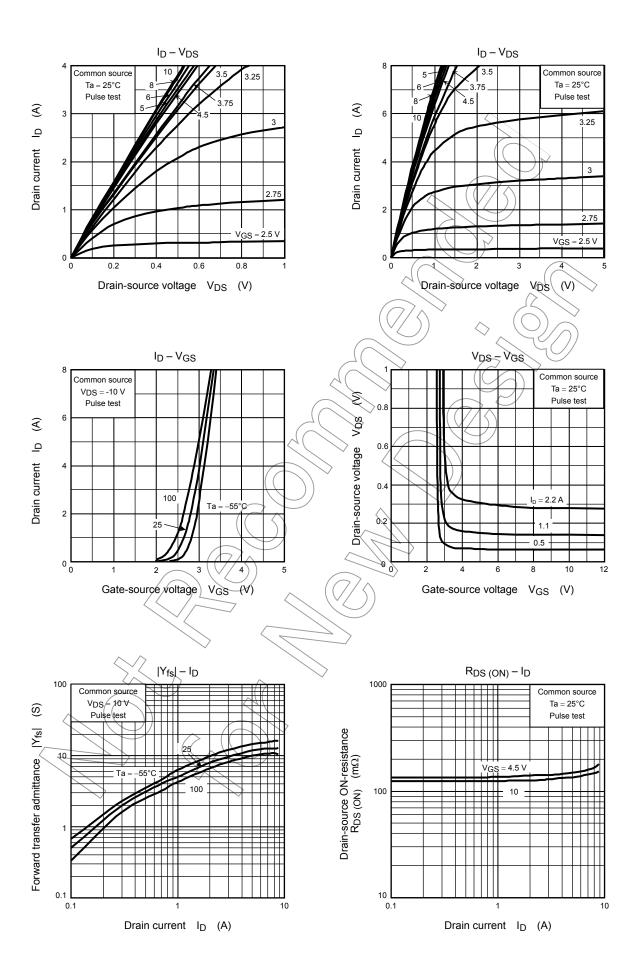
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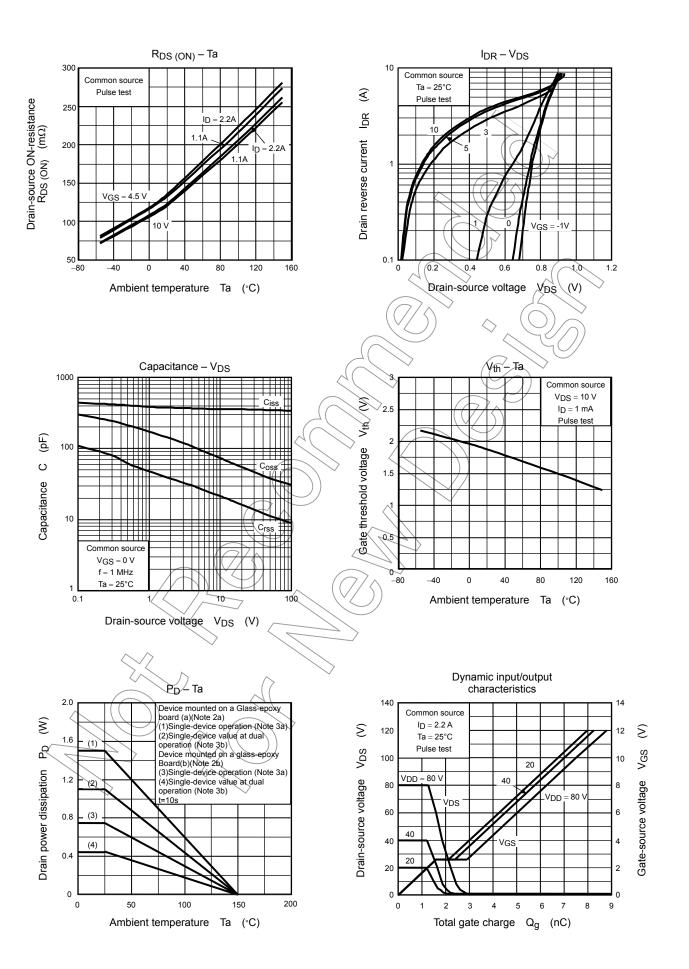
## Electrical Characteristics (Ta = 25°C)

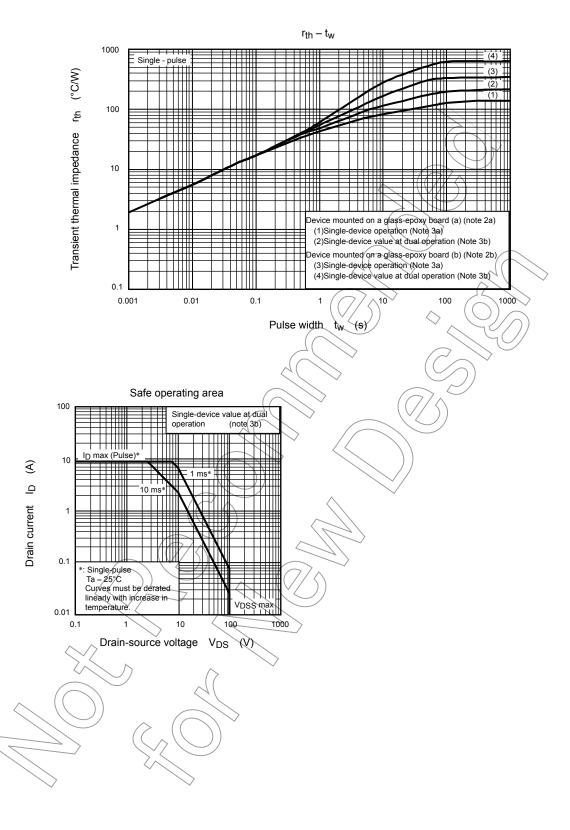
Chara	acteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	urrent	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V	_	_	±10	μΑ
Drain cutoff curr	rent	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	_	_	10	μΑ
Drain-source b	roakdown voltago	V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	100	_	_	V
Drain-source breakdown voltage		V (BR) DSX	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	60		_	
Gate threshold	voltage	V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	(1)	) >-	2.3	V
Drain-source ON-resistance		R <sub>DS (ON)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.1 A	) <	140	190	mΩ
		R <sub>DS</sub> (ON)	V <sub>GS</sub> = 10 V , I <sub>D</sub> = 1.1 A	$\rightarrow$	130	180	11122
Forward transfe	r admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 10 V , I <sub>D</sub> = 1.1 A	2.7	5.4	_	S
Input capacitance		C <sub>iss</sub>		_	360	_	
Reverse transfer capacitance		C <sub>rss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	22	_	pF
Output capacitance		Coss		- /	75	$\overline{\mathcal{D}}$	
Switching time	Rise time	t <sub>r</sub>	10 V D _ 10 = 1.1 A	(	7	> _	
	Turn-on time	t <sub>on</sub>	V <sub>GS</sub> 10 V		> 14	_	20
	Fall time	t <sub>f</sub>	V <sub>DD</sub> ≈ 50 V		3	_	ns
	Turn-off time	t <sub>off</sub>	Duty ≨ 1%, t <sub>W</sub> = 10 μs	_	17	_	
Total gate charge (gate-source plus gate-drain)		Q <sub>g</sub> (	$V_{DD} \ge 80 \text{ V}, V_{GS} = 10 \text{ V}, V_{D} = 2.2 \text{ A}$	_	7.5	_	
(Note 7)			$V_{DD} = 80 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 2.2 \text{ A}$	_	4.5	_	
Gate-source charge 1		Q <sub>gS1</sub>		_	1.6		nC
Gate-drain ("Miller") charge		Qgd	$V_{DD} \simeq 80 \text{ V}, V_{GS} = 10 \text{ V}, D = 2.2 \text{ A}$	_	1.3	_	
Gate switch charge		Qsw		_	2.0	_	

## Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain reverse current Pulse (Note 1)	I <sub>DRP</sub>	_	_	_	8.8	Α
Forward voltage (diode)	VDSF	I <sub>DR</sub> = 2.2 A, V <sub>GS</sub> = 0 V	_	_	-1.2	V







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