Silicon N-Channel MOS FET

# HITACHI

ADE-208-1352 (Z) 1st. Edition Mar. 2001

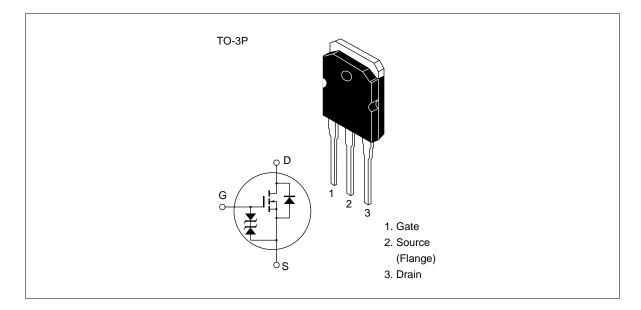
## Application

Low frequency power amplifier Complementary pair with 2SJ351, 2SJ352

### Features

- High power gain
- Excellent frequency response
- High speed switching
- Wide area of safe operation
- Enhancement-mode
- Good complementary characteristics
- Equipped with gate protection diodes

## Outline





## **Absolute Maximum Ratings** (Ta = 25°C)

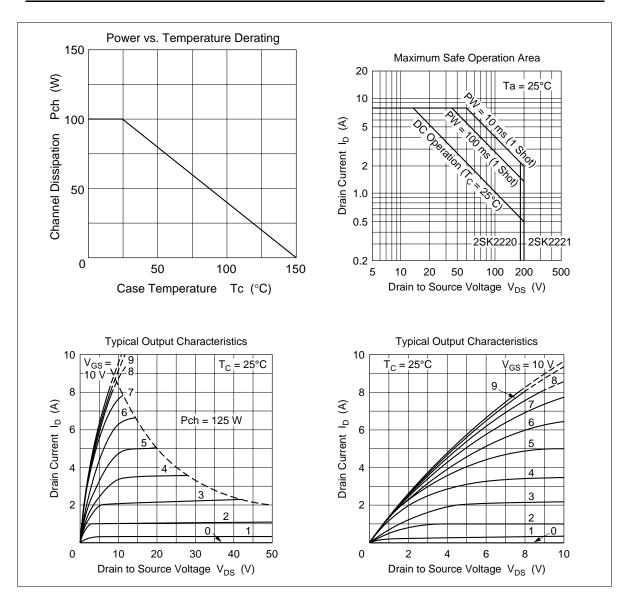
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK2220	V <sub>DSX</sub>	180	V
	2SK2221		200	
Gate to source voltage		V <sub>GSS</sub>	±20	V
Drain current		I <sub>D</sub>	8	А
Body to drain diode reverse drain current		I <sub>DR</sub>	8	А
Channel dissipation	Pch*1	100	W	
Channel temperature		Tch	150	°C
Storage temperature		Tstg	-55 to +150	°C

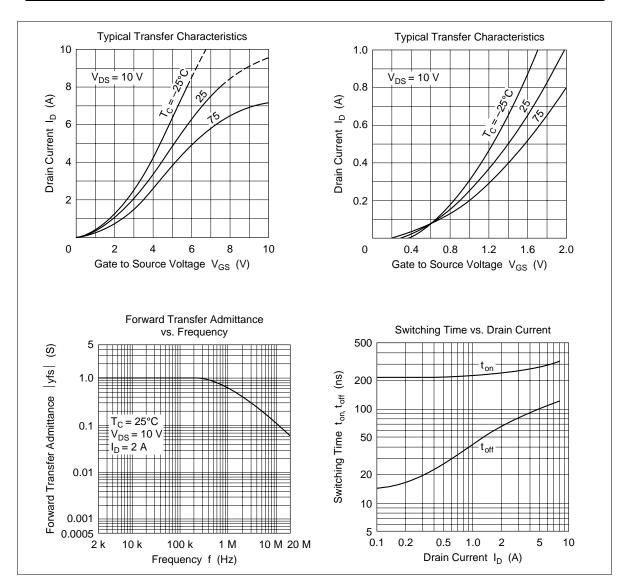
Note 1. Value at Tc =  $25 \degree C$ 

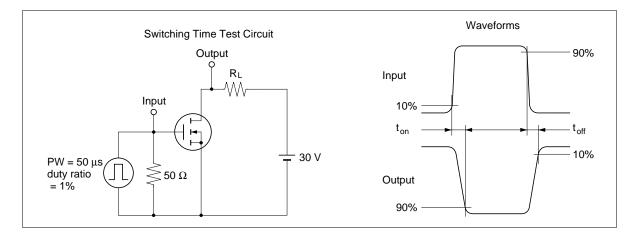
# **Electrical Characteristics** (Ta = 25°C)

Item		Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source	2SK2220	V <sub>(BR)DSX</sub>	180	_	—	V	$I_{\rm D} = 10 \text{ mA}, V_{\rm GS} = -10 \text{ V}$
breakdown voltage	2SK2221	_	200	_	_		
Gate to source by voltage	reakdown	$V_{(BR)GSS}$	±20	—	—	V	$I_{G} = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source cu	utoff voltage	$V_{\text{GS(off)}}$	0.15	_	1.45	V	I <sub>D</sub> = 100 mA V <sub>DS</sub> = 10 V
Drain to source s voltage	aturation	$V_{\text{DS(sat)}}$	_	_	12	V	$I_{D} = 8 \text{ A}, \text{ V}_{GD} = 0 \text{ V}^{*1}$
Forward transfer	admittance	y <sub>fs</sub>	0.7	1.0	1.4	S	$I_{D} = 3 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	)	Ciss	_	600	—	pF	$V_{GS} = -5 V$
Output capacitan	се	Coss	—	800	—	pF	$V_{DS} = 10 V$
Reverse transfer	capacitance	Crss	_	8	—	pF	f = 1 MHz
Turn-on time		t <sub>on</sub>	—	250	_	ns	V <sub>DD</sub> = 30 V
Turn-off time		t <sub>off</sub>	_	90	_	ns	$I_{D} = 4 \text{ A}$

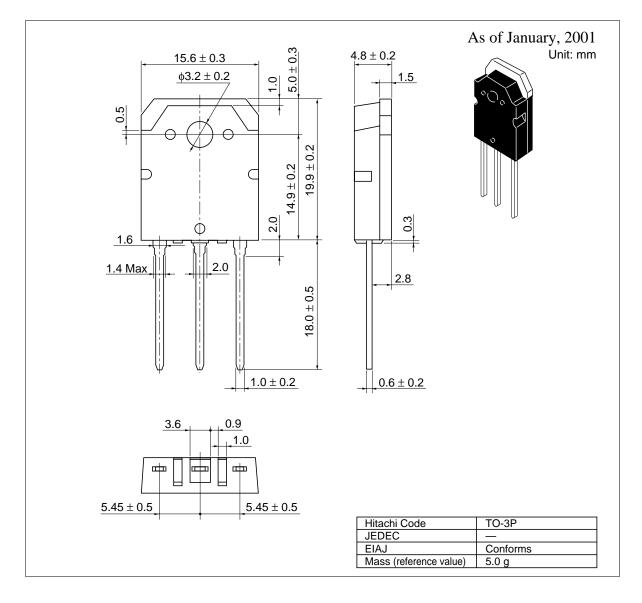
Note 1. Pulse Test







### **Package Dimensions**



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